TLE 6270 R

Quad Low Side Injector Driver

TLE6270R

Data Sheet

Rev.1.3.1, 2011-06-27

Automotive Power

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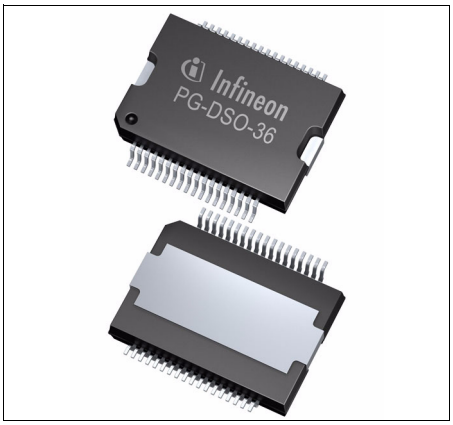
1 Overview



PG-DSO-36

Features

- Four integrated Low Side Switches, control logic and -outputs for external High Side Switches
- Programmable Peak and Hold output current control to adapt to application requirements.
- Detailed diagnostic of defective or missing injector connections
- Serial Peripheral Interface (SPI) for diagnostics and control of the device
- Short Circuit-, ESD and Overtemperature Protection
- Undervoltage Reset
- Green Product (RoHs compliant)
- AEC Qualified

Application

- Gasoline Direct Injection

General Description

TLE6270R is specially suited for Gasoline Direct Injection Systems in Automotive Applications. The device controls the external High Side Transistors to supply the injectors alternating with battery Voltage and a boosted high voltage according the requirement of the applied injectors. The device incorporates the Low Side driver Transistors for four Injector Channels.

Product Summary

Parameter	Symbol	Value	Unit
Output channels		4	
Continuous output voltage max.	V_{OUT}	80	V
Clamping voltage typ.	V_{CLP}	87	V
Peak current typ.	I_{P_C}	11.50	A
Hold current typ.	I_H	2.30	A
On resistance max. at 150 °C	R_{ON}	300	mΩ

Type	Package	Marking
TLE6270R	PG-DSO-36	TLE6270R

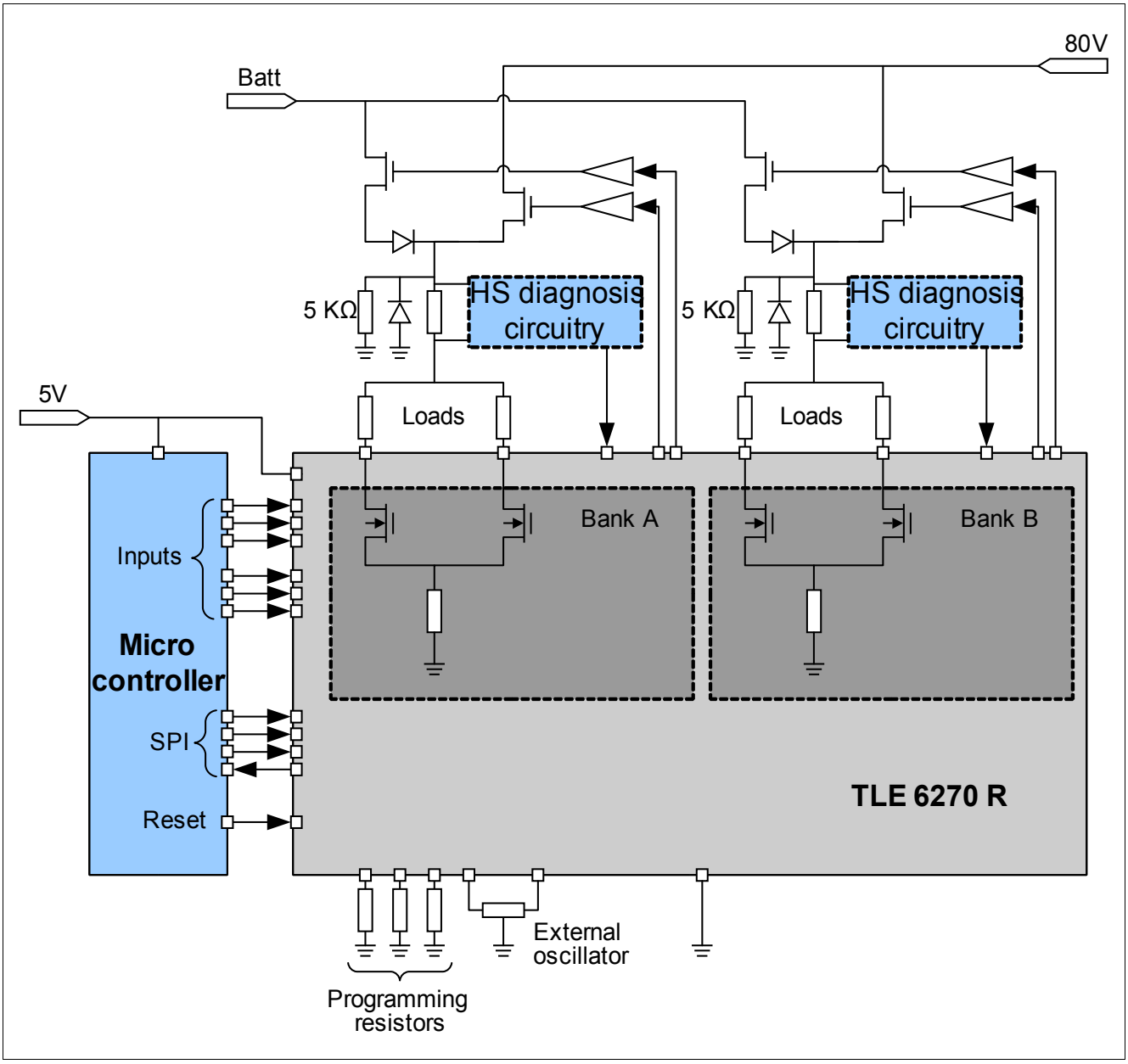


Figure 1 Application Diagram

2 Block Diagram

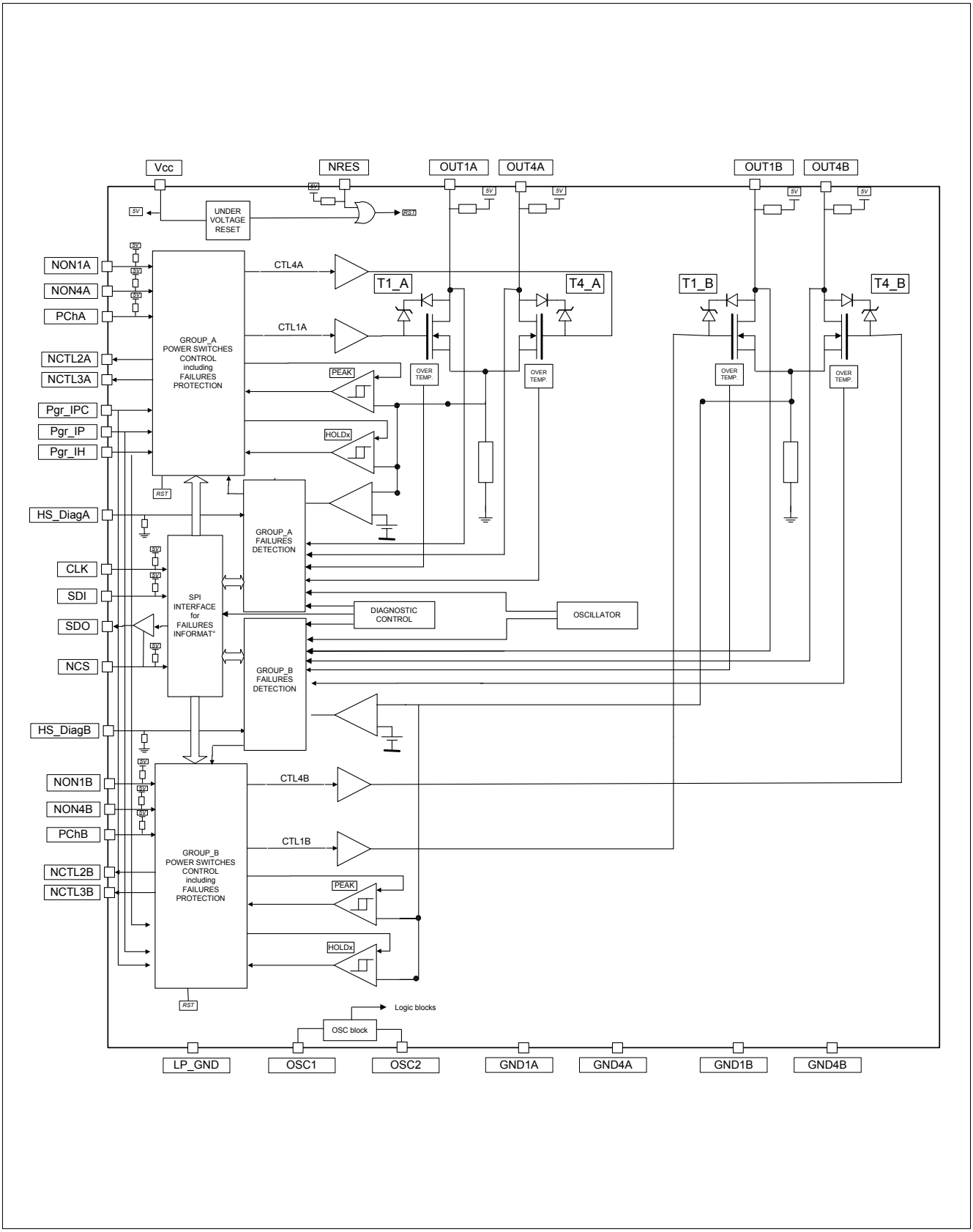


Figure 2 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

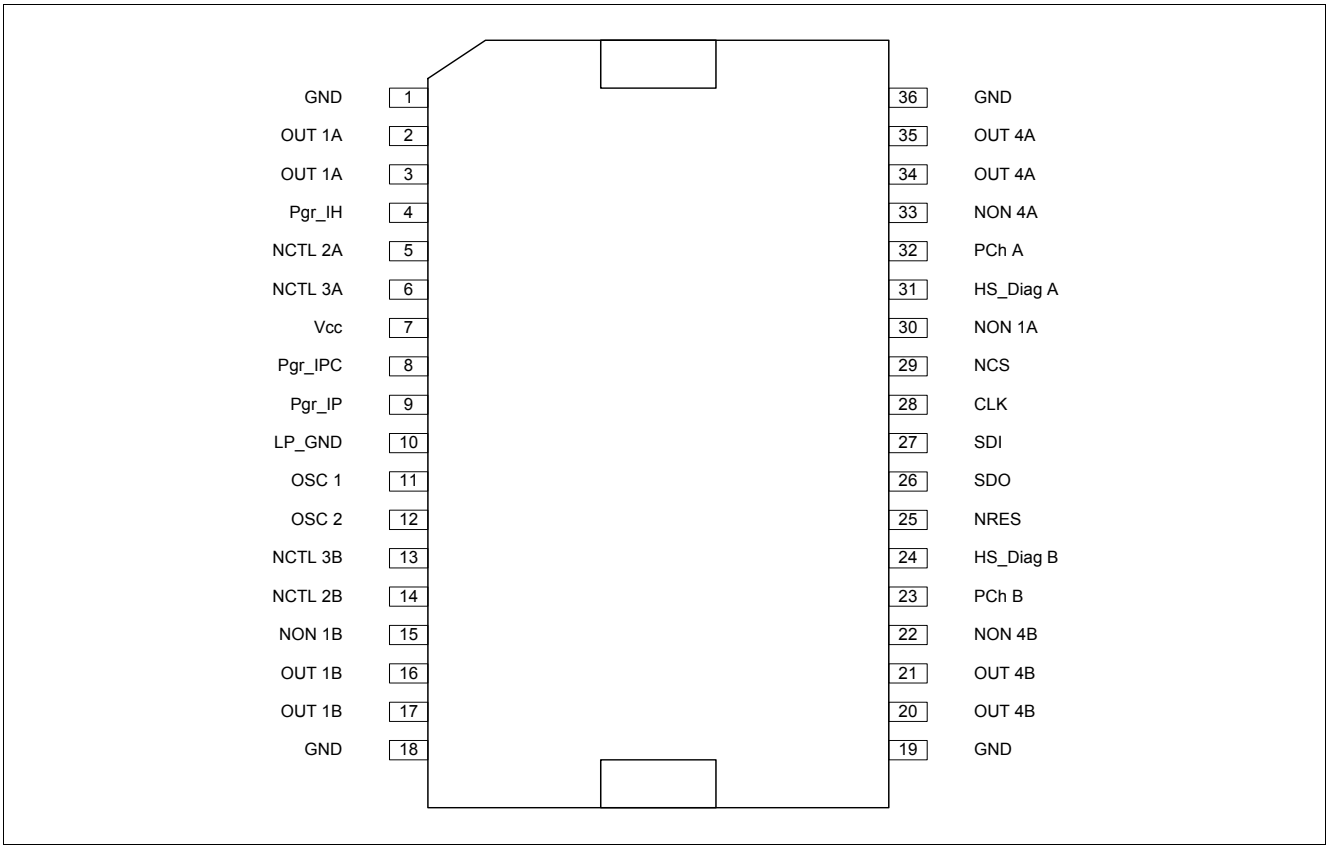


Figure 3 Pin Configuration P-DSO-36

3.2 Pin Definitions and Functions

Pin	Symbol	Function
7	V_{CC}	5 V Power Supply
10	LPGND	Low Power Ground
1	GND	High Power Ground
18	GND	High Power Ground
19	GND	High Power Ground
36	GND	High Power Ground
2	OUT1A	OUTPUT channel 1A
3	OUT1A	OUTPUT channel 1A
34	OUT4A	OUTPUT channel 4A
35	OUT4A	OUTPUT channel 4A
16	OUT1B	OUTPUT channel 1B
17	OUT1B	OUTPUT channel 1B
20	OUT4B	OUTPUT channel 4B
21	OUT4B	OUTPUT channel 4B
30	NON1A	Control input channel 1A
33	NON4A	Control input channel 4A
15	NON1B	Control input channel 1B
22	NON4B	Control input channel 4B
32	PChA	Pre-charge input group A
23	PChB	Pre-charge input group B
8	Pgr_IPC	IPC programming input[1)]
9	Pgr_IP	IP programming input
4	Pgr_IH	IH programming input
5	NCTL2A	Control output high side 2A
6	NCTL3A	Control output high side 3A
14	NCTL2B	Control output high side 2B
13	NCTL3B	Control output high side 3B
31	HS_Diag A	High side diagnostic input A
24	HS_Diag B	High side diagnostic input B
25	NRES	Reset input
27	SDI	Serial Data Input
26	SDO	Serial Data Output
28	CLK	Clock input for serial interface
29	NCS	Chip-select input
11	OSC1	External resonator input
12	OSC2	External resonator output
–	Case	*Note: Has to be connected to GND on the PCB*

1) If there is no pre-charge resistor this pin has to be connected to V_{CC} on the PCB

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_J = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.1.1	Supply voltage	V_{CC}	-0.3	7	V	–
Outputs						
4.1.2	Continuous output voltage	V_{OUT}	-1.5	80	V	–
4.1.3	Continuous output current, one output active	I_{OUTC}	-5	5	A	–
4.1.4	Peak output current	I_{OUTP}	-10	20	A	see **Chapter 5.5**
4.1.5	Clamping energy repetitive pulse	W_{OFFr}	–	30	mJ	all T°, see **Figure 4**
4.1.6	Clamping energy single pulse	W_{OFFs}	–	130	mJ	all T°, see **Figure 4**
Inputs and NCTL, SDO outputs						
4.1.7	Continuous voltage	V_{IN}	-0.3	7	V	–
All pins						
ESD Susceptibility						
4.1.8	Electrostatic discharge	V_{ESD}	-2000	2000	V	R = 1.5 kΩ; C = 100 pF; HBM[2)]
Operating Range						
4.1.9	Operating Temperature Range	T_J	-40	150	°C	1)
4.1.10	Storage Temperature Range	T_J	-55	150	°C	1)

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to EIA/JESD 22-A114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

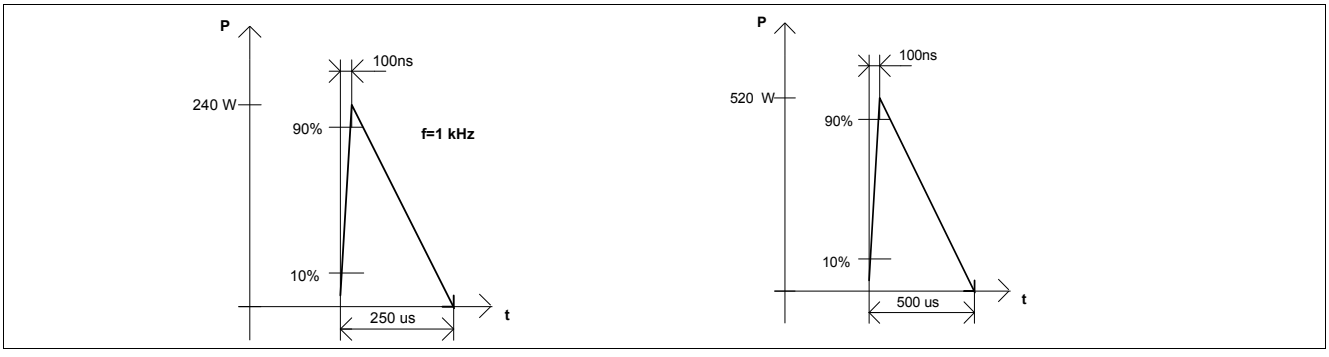


Figure 4 Energy Repetitive Pulse and Energy Single Pulse

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage	V_S	4.5	5.5	V	–
4.2.2	Junction temperature continuous	T_{j1}	-40	150	°C	Permanent operation

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	–	2	K/W	–

1) Not subject to production test, specified by design.

5 Functional Description

5.1 List of Functionalities

The device performs the following functionalities:

- Load control
  - 4 low side power transistors driven by 4 parallel CMOS compatible inputs.
- Output current control
  - output current comparators and logic circuit to generate high side switches control signals NCTL2 and NCTL3.
  - current thresholds programmable by external resistor.
- Diagnostic of defective or missing injector connections and overtemperature
  - comparators and logic circuit to interpret unexpected current, voltages and HSDiag input status as short circuit or disconnection of the injector.
  - 4 thermal sensors for independent overtemperature detection on the 4 channels.
- Protection
  - all inputs/outputs: protection against ESD (all input and output pins)
  - T1, T4, internal power transistors: protection against overvoltage and Transients (Schaffner test pulses)…
  - external transistors connected via NCTL2 and CLT3: protection against overvoltage and Transients (Schaffner test pulses)…
- Reset
  - external reset (reset pin)
  - internal reset (undervoltage reset)
- Electro Magnetic Compatibility (EMC)

These functionalities are described in the next chapters.

5.2 Load Control

Each output transistor is switched on and off by an individual control signal (NON input).

In normal operation, when NON is low, the transistor is ON and when NON is high the transistor is OFF. Also after power up, the outputs must have the status defined by the NON input.

The logic level of the input is CMOS compatible.

As there is an internal pull-up, the output transistor is switched off when the input is not connected.

It is possible to drive two separate loads simultaneously as far as they do not belong to the same bank.

5.3 Output Current Control

From the output current comparators and inputs signals, a logic circuit controls the 4 current levels IPC, IP, IH and ID by commanding the high side drivers T2 and T3 via NCTL2 and NCTL3 (see **Chapter 8**). T2 and T3 are OFF when NCTL2 and NCTL3 are at high level.

- IPC level is controlled between high and low values
  IPC value can be programmed through Pgr_IPC pin
- IP level
  the transition from IPC to IP is controlled by PCh pin
  IP value can be programmed through Pgr_IP pin
- IH level is controlled between high and low values
  the transition from IP to IH starts when peak level is reached
  IH value can be programmed through Pgr_IH pin
- ID level is controlled between high and low values. ID is equal to IH.
  the transition from IH to ID is controlled by NON1 or NON4 and PCh pins
  the damp pulse is not present if there is no damp pulse command at NON1/4
- Currents values according to programming resistors (see also graph in **Chapter 7**)
  – R_Pgr_IP = k_P / IP
  – R_Pgr_IPC = k_{PC} / IPC
  – R_Pgr_IH = k_H / IH

The theoretical Design calculation leads to k_P = 140000 = 8 × k_{PC} = 4 × k_H.

Note: If Pgr_IPC pin has no resistor and is connected to V_{CC} then there is no pre-charge and no damping. Then the Pch signal is not used and the output is controlled directly by the NON input.

Current Control Configurations according to NON and Pch Signals

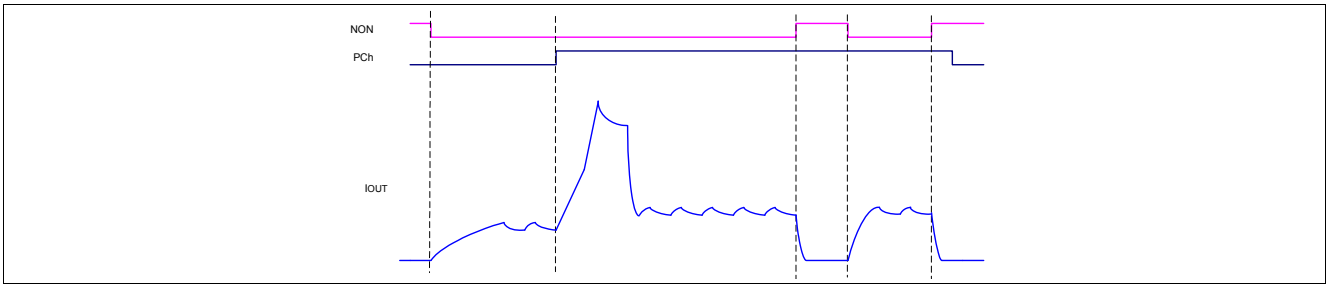


Figure 5 Pre-charge → Peak → Hold → Damp

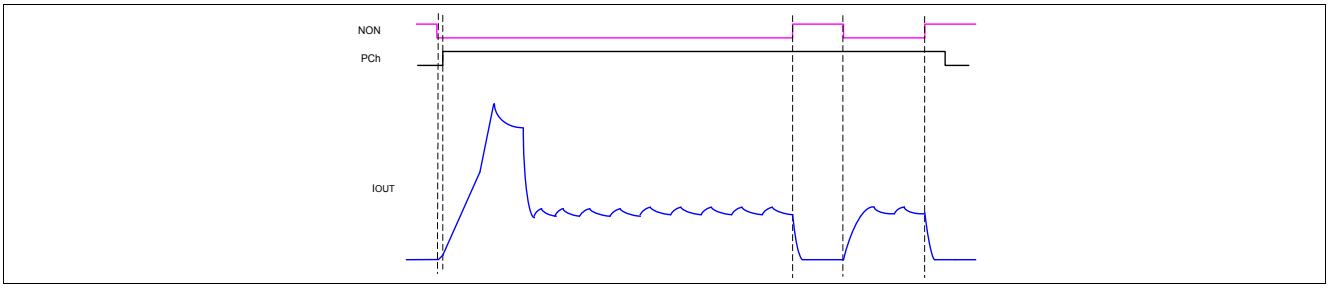


Figure 6 Peak → Hold → Damp

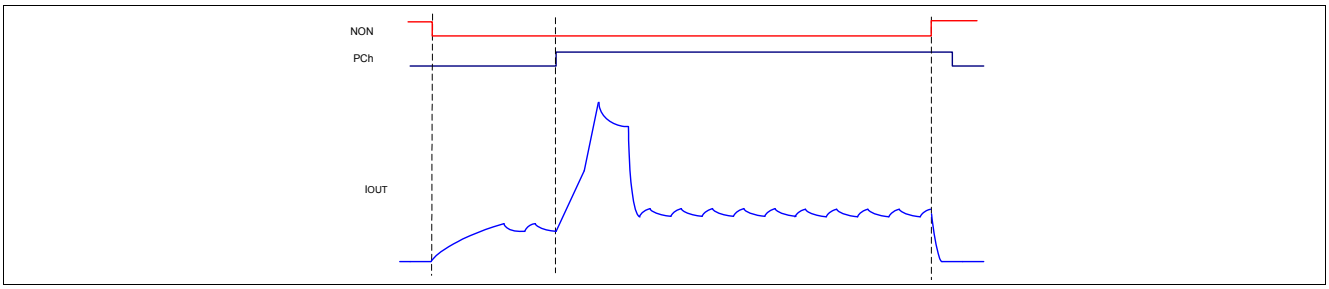


Figure 7 Pre-charge → Peak → Hold

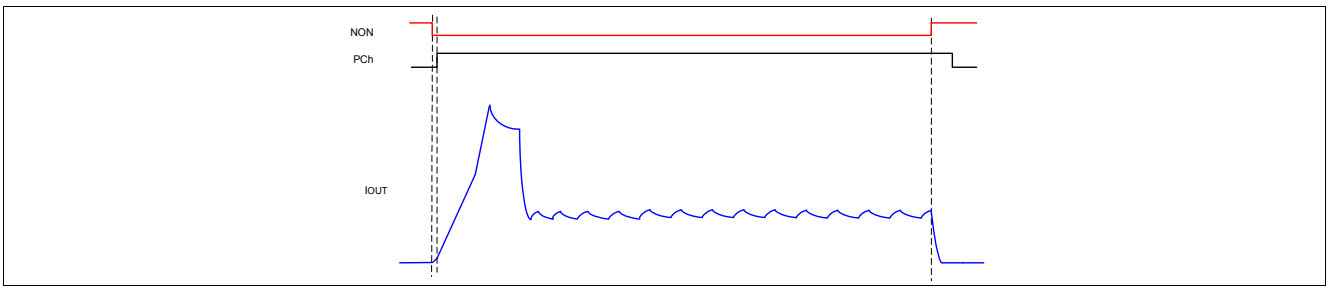


Figure 8 Peak - Hold

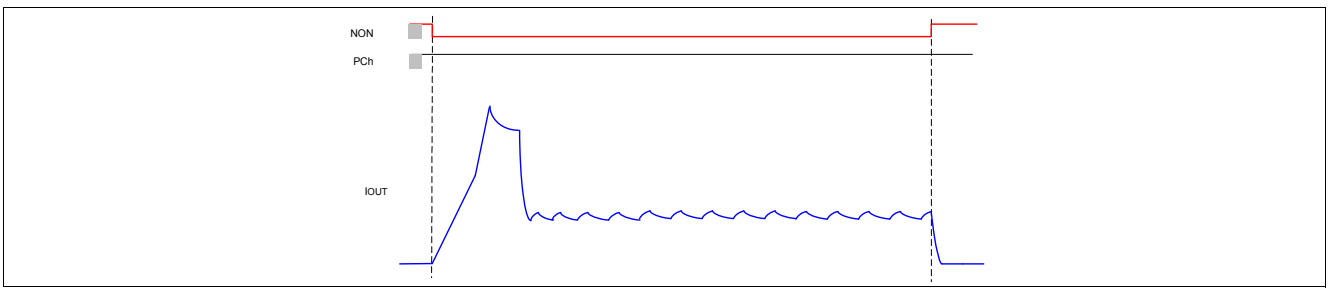


Figure 9 Peak - Hold, if Pgr_IPC pin has no resistor and is connected to V_{CC}

5.4 Diagnostic

The TLE6270R detects too high output current and too short or too long time to reach the peak current in ON state, too high output voltage in OFF state. It is also informed of too high current in the high side transistors via the HS_Diag pin.

According to these comparator outputs and the NON signals, a logic circuit defines the failures (failure detection).

When the failure is dangerous for the ECU, the engine management system, the vehicle or the car driver, all transistors T1, T2, T3, T4 are immediately switched off for protection (failure protection).

Then, for limp home and for repairing, the failures are read by the microcontroller via SPI (failure information).

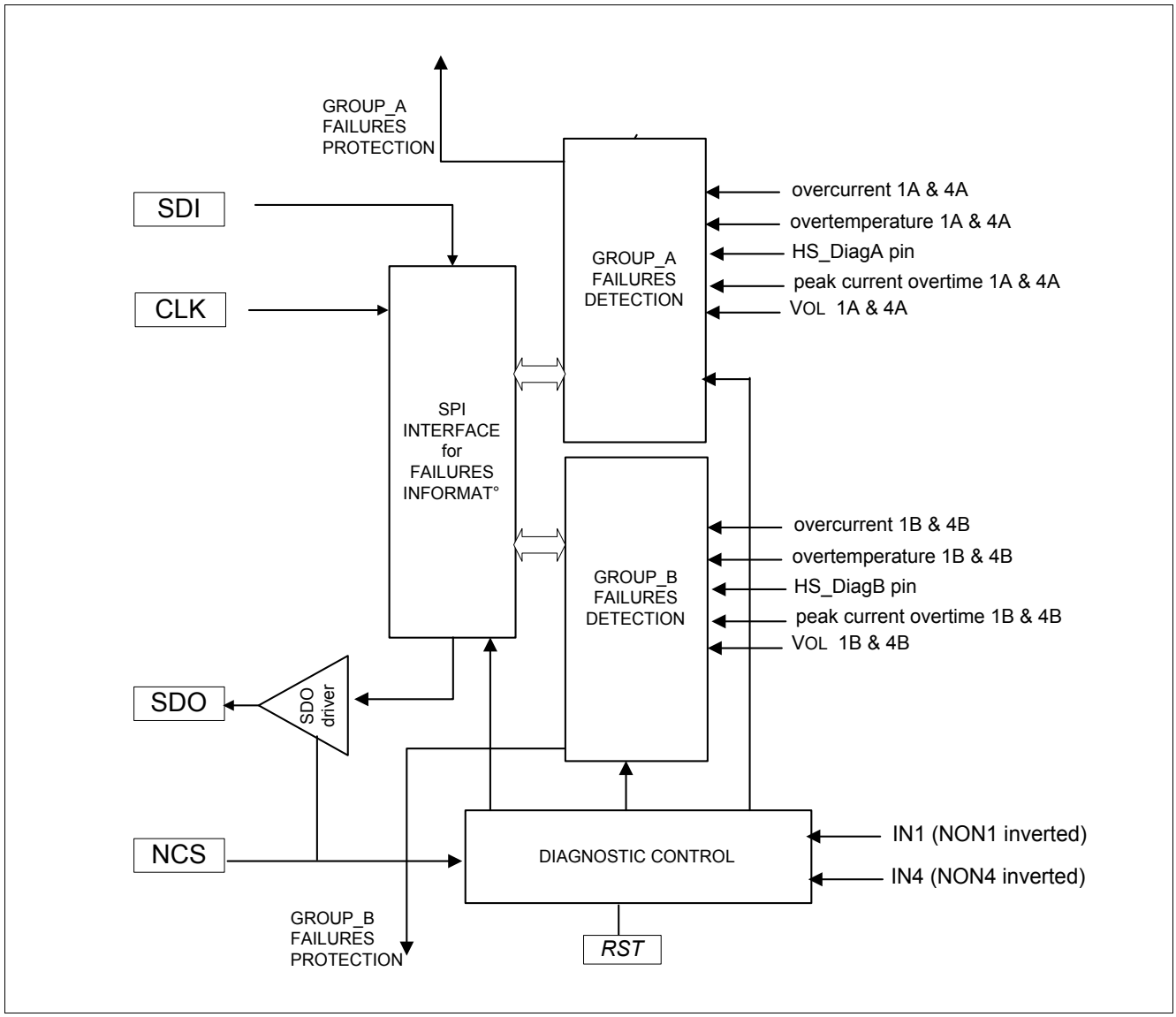


Figure 10 Diagnostic Schematic

5.4.1 Failures Detection

For information only: Table 1 describes for each problem the detection mode and the failure detected (for exact detail, see Table 2).

Table 1 Failures Detection

Connector Point	Problem	Failure Detection Mode	Failures Detected
HS	HS short to battery	HS_Diag L → H or OUT1/4 peak current overtime	INJ1_SC and INJ4_SC
	HS short to ground	HS_Diag L → H or OUT1/4 peak current overtime	INJ1_SC and INJ4_SC
	HS open circuit	peak overtime and OUT1/4 OFF overvoltage	INJ1_OL and INJ4_OL
LS1	LS1 short to battery	OUT1 overcurrent	INJ1_SC
	T1 overtemperature	OUT1 overtemperature	INJ1_SC
	LS1 short to ground	HS_Diag L → H or OUT1 peak current overtime	INJ1_SC
	LS1 short to HS	OUT1 overcurrent or peak current undertime	INJ1_SC
	LS1 open circuit	peak overtime and OUT1 OFF overvoltage	INJ1_OL
LS4	LS4 short to battery	OUT4 overcurrent	INJ4_SC
	T4 overtemp	OUT4 overtemperature	INJ4_SC
	LS4 short to ground	HS_Diag L → H or OUT4 peak current overtime	INJ4_SC
	LS4 short to HS	OUT4 overcurrent or peak current undertime	INJ4_SC
	LS4 open circuit	peak overtime and OUT4 OFF overvoltage	INJ4_OL

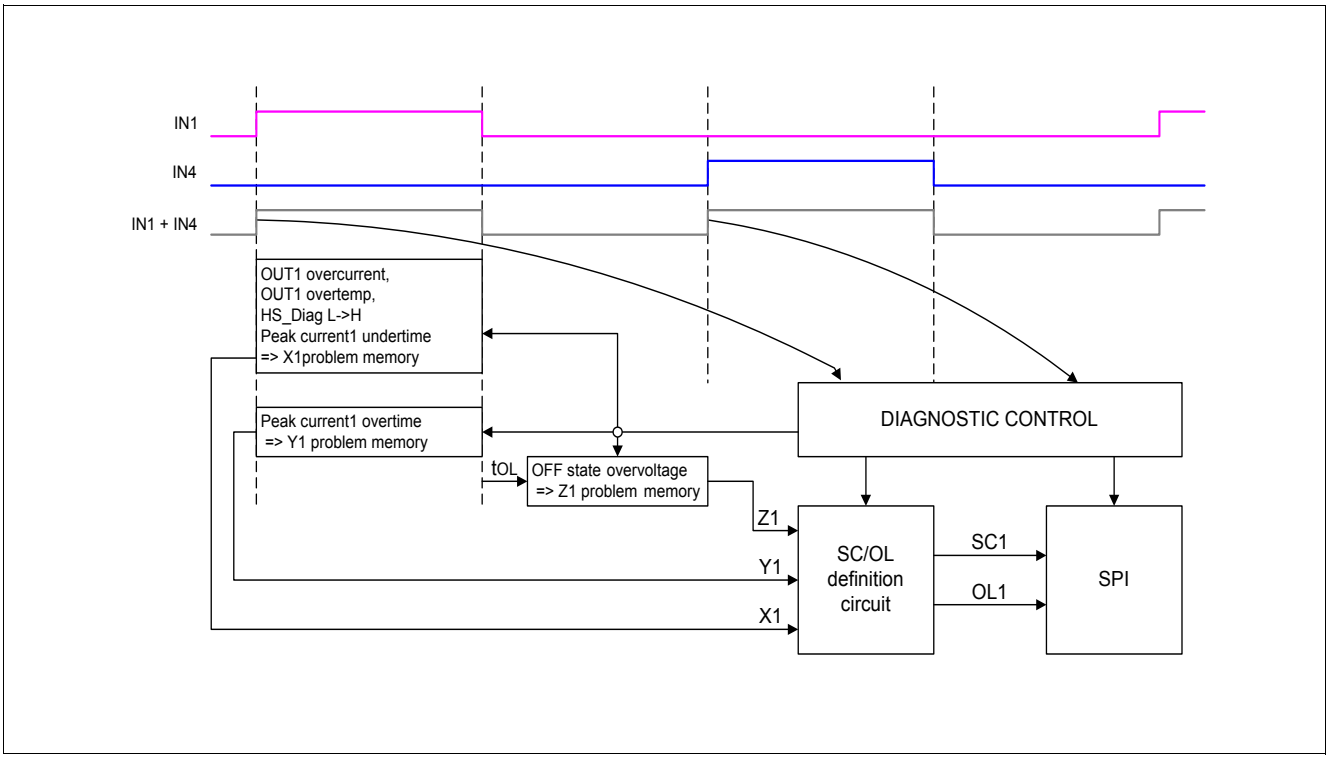


Figure 11 Diagram of INJ1 Failures Detection

OFF State open load Functionality

The TLE6270GR is able to detect a missing load in OFF-state using a pull-up resistor connected at the output when the both outputs of the correspoding bank are turned off.

For the correct functionality of this feature a 5KΩ resistor has to be connected in parallel with the freewheeling diode of each bank.

OFF State Overvoltage Functionality:

- Comparator:
  - There is one comparator for two channels. A low level on the comparator output (called VOFF) means no failure.
  - The voltage on OUT1 (resp. OUT4) is checked at the OFF state between OUT1 and OUT4 ON states (resp. between OUT4 and OUT1 ON states).
- Filter time: For OUT1 (resp. OUT4), the filter time starts:
  - at H → L transition on IN1 (resp. IN4)
  - if V_{OFF} is high when this first filter time is finished
  - at every L → H transition on V_{OFF}

HS Diag Filter Functionality:

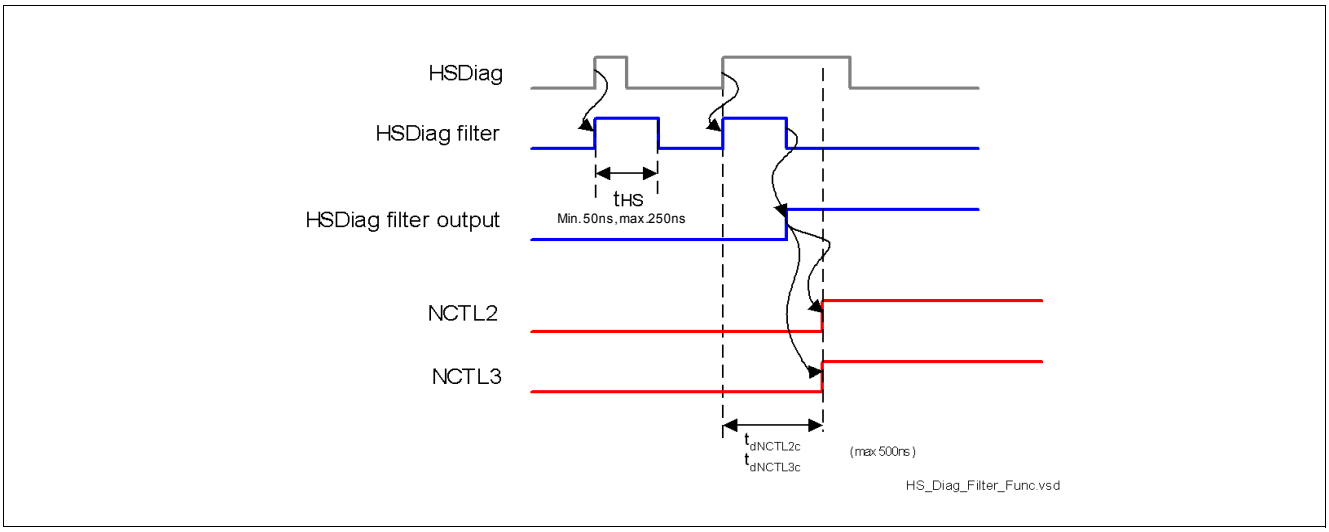


Figure 12 HS Diag Filter Functionality (optionally only one out of NCTL2 or NCTL3 can be on at the same time)

Diagnostic Control Circuit Functionality:

The SC1 (resp.4) and OL1 (resp.4) failures are transferred in the SPI on IN1 and IN4 positive edges. Just after, the X1, Y1, Z1 (resp. X4, Y4, Z4) problem memories are reset.

SCn/OLn Definition Circuit Table:

Table 2 SC/OL Definition Circuit

valid for n=1 or n=4

Memories			Failures	
Xn	**Yn**	**Zn**	**SCn**	**OLn**
0	0	0	0	0
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

5.4.2 Failures Information (via SPI)

The failures detected are communicated to the microcontroller via a Serial/Peripheral Interface (SPI) in order to minimize the pin number.

The SPI contains a failure register, a coder, a shift register, and a SDO driver:

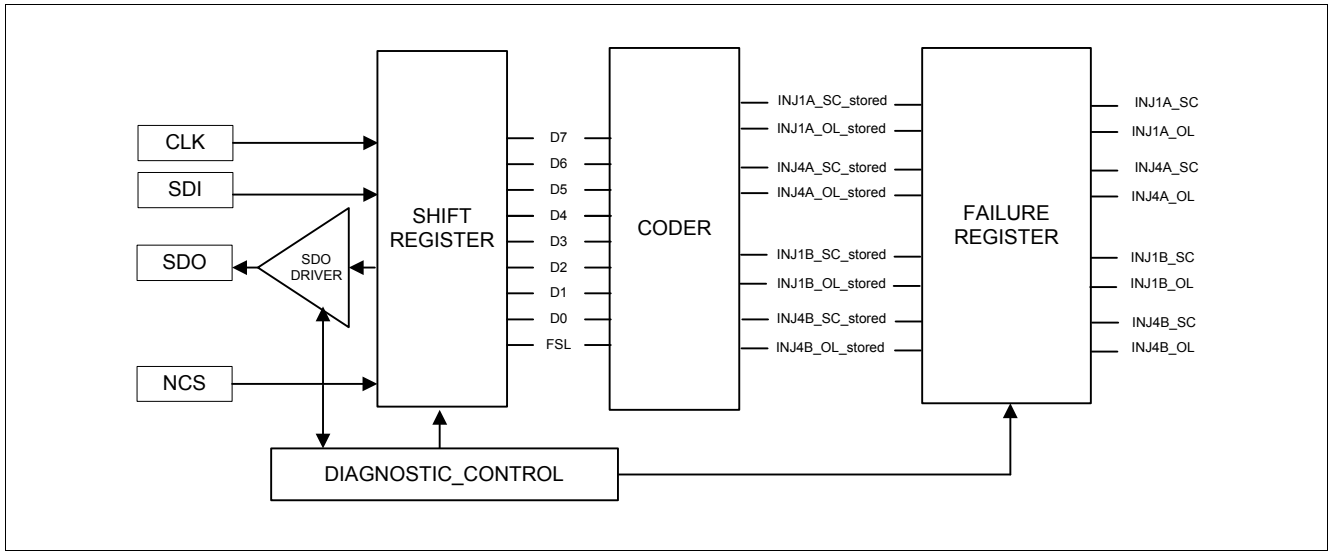


Figure 13 Failures Information

Failure Register

Each failure is stored in an individual register (this cannot be done directly in the shift register because a failure can occur while the shift register is being read).

If the failure occurs, it remains until the SPI is read.

The failure register is cleared when the SPI is read (FR_CLEAR signal).

Output Coder

The SC and OL failures of the 4 outputs are coded on an 8 bit word described hereafter:

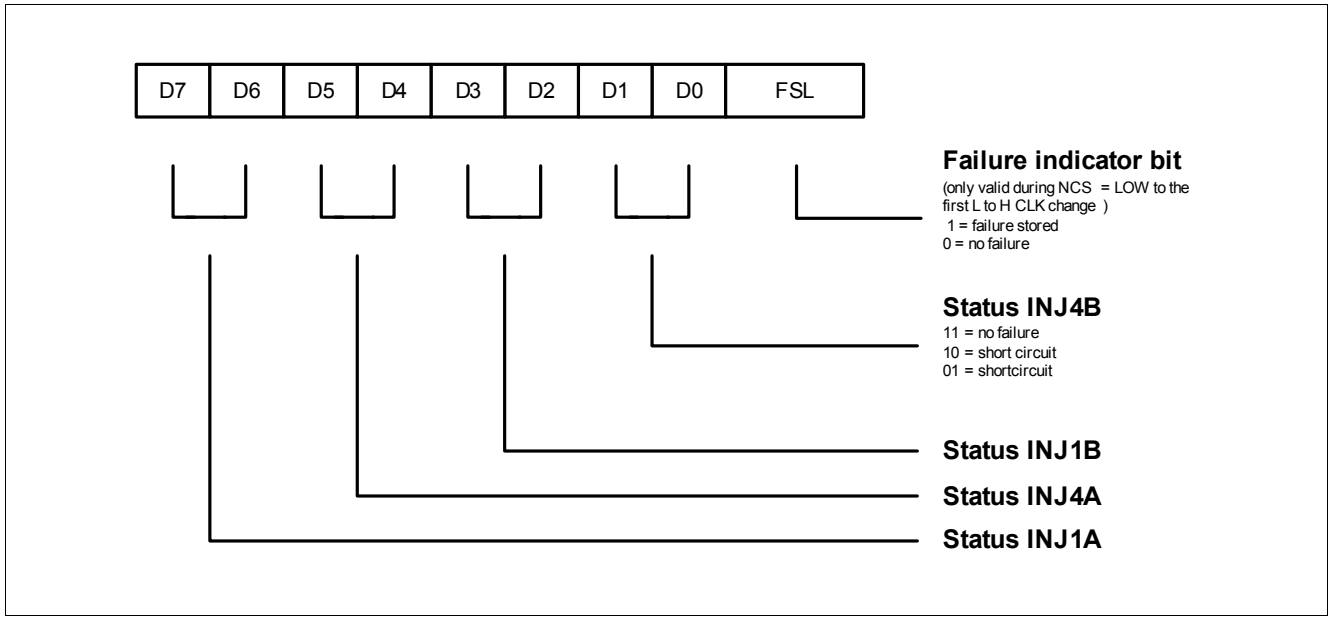


Figure 14 Output Coder

Table 3 Failures Coding and Priorities

valid for i=0 or i=2 or i=4 or i=6

Failure		SPI Bits		
SC	**OL**	**FSL**	**Di+1**	**Di**
0	0	0	1	1
0	1	1	0	1
1	0	1	1	0
1	1	1	1	0

The first bit of the shift register (FSL) is set to high level if there is a failure stored in the failure register.

Input Coder

t_1 and t_2 times are coded on 3 bit and 5 bit respectively as described hereafter:

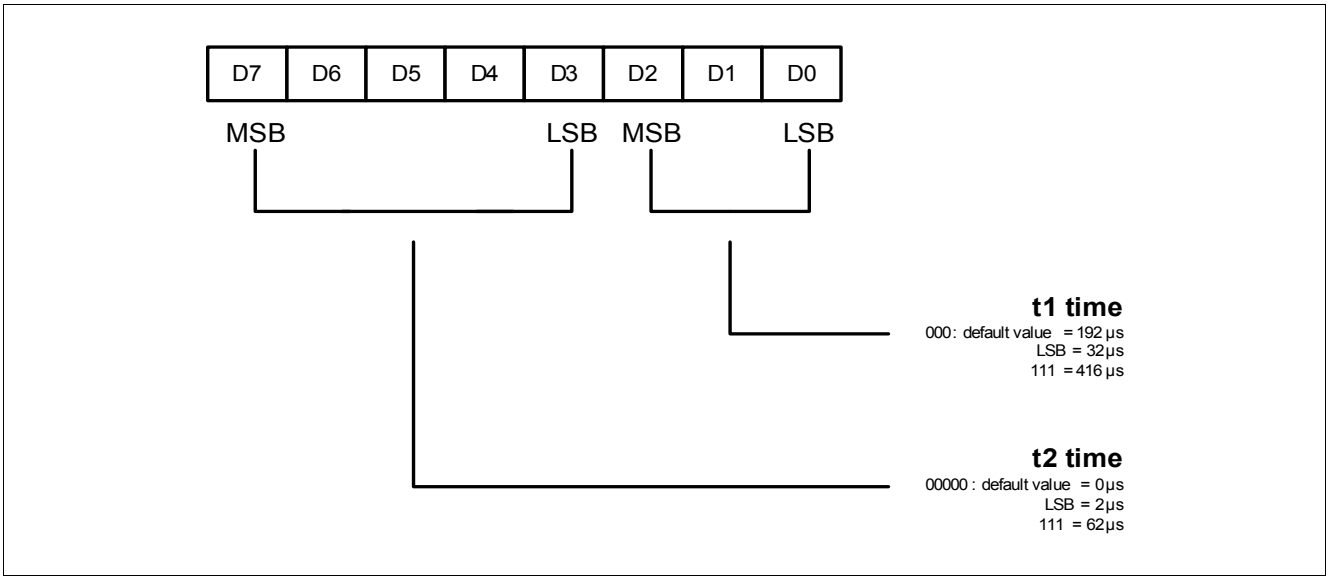


Figure 15 Input Coder

Table 4 describes the time coding:

Table 4 Time Coding

D7	D6	D5	D4	D3	D2	D1	D0	Time
X	X	X	X	X	0	0	0	t_1 = 192 µs
X	X	X	X	X	0	0	1	t_1 = 224 µs
…								…
X	X	X	X	X	1	1	1	t_1 = 416 µs
0	0	0	0	0	X	X	X	t_2 = 0 µs
0	0	0	0	1	X	X	X	t_2 = 2 µs
…								…
1	1	1	1	1	X	X	X	t_2 = 62 µs

Shift Register

The serial output of the diagnostic shift register is SDO. The serial input is SDI.

With the H/L change on NCS the first bit of the diagnostic shift register is transmitted to the SDO output.

The CLK pin clocks the diagnostic shift register. New SDO data will appear on every CLK's rising edge and new SDI data will be latched into the shift register on every CLK's falling edge.

With the first positive pulse of the CLK the failure register will be cleared by FR_CLEAR.

There is no bus collision at a small spike at the NCS. The CLK is always LOW, while the NCS signal is changing.

SPI Control

The SPI control block monitors the data transfer from failure register to shift register and clear these register.

This is done with the FR_SR_TRANS and FR_CLEAR signals as described in the following diagram:

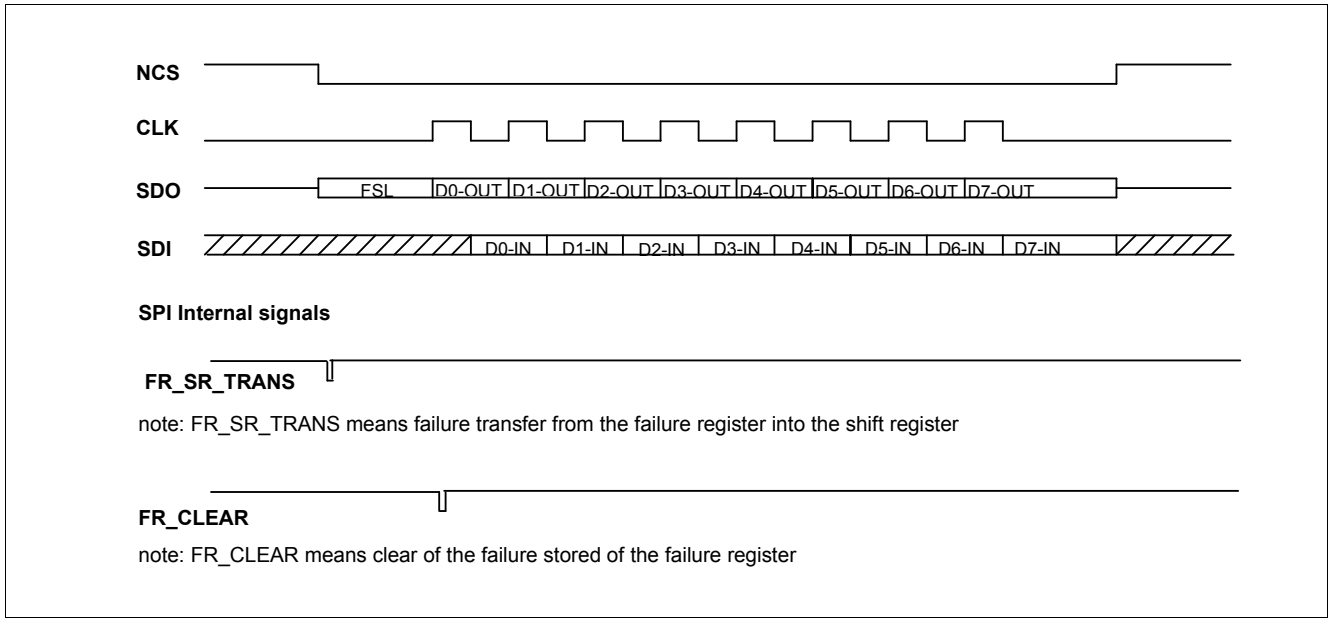


Figure 16 SPI Control

SDO Driver

The SDO driver drives the data on the diagnostic line.

SDO is tri-stated when NCS is high.

5.5 Protections

5.5.1 All Inputs/Outputs

All pins are protected against ESD 2kV Human body model.

5.5.2 T1, T4 Power Transistors

- Protection against damaging failures

Table 5 Protection against Damaging Failures

Problem detected	Transistors switched off
T1 or T4 overcurrent	T1, T4 (internally) and T2, T3 (via NCTL2, NCTL3)
T1 or T4 overtemperature	T1, T4 (internally) and T2, T3 (via NCTL2, NCTL3)
HS_Diag L → H	T1, T4 (internally) and T2, T3 (via NCTL2, NCTL3)
T1 or T4 peak current undertime	T1, T4 (internally) and T2, T3 (via NCTL2, NCTL3)
T1 or T4 peak current overtime	T1, T4 (internally) and T2, T3 (via NCTL2, NCTL3) and t_2 starts.

Note: The protection latches are reset when the NON input is at high level.

- Protection against overvoltage
  A clamping circuit limits the output voltage to a defined value (V_{clp}) in order to avoid the breakdown of the output transistor when the solenoid load is switched off.
- Protection against turn on due to fast voltage ramp on output.
  A very fast voltage slope on the output can turn on the power transistor (capacitive effects) especially when the normal gate pull-down structure is not active (IC not supplied, V_{CC} too low …). In this case, the transistor is turned off immediately. This function is guaranteed for V_{CC} between 0 and 5.5 V.

5.6 Reset

There are two different reset functions:

- Undervoltage reset
- NRES reset pin

If one or several of the following conditions are present:

- V_{CC} lower than V_{CCRES},
- NRES pin at low level,

the low side T1, T4 are switched off, NCTL2 and NCTL3 set to high level, all diagnostic registers are reset and the SDO is tri-stated.

6 Electrical Characteristics

6.1 Supply Current

Electrical Characteristics: Supply Current

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Standby current	I_{CC_STB}	–	–	10	mA	without load
6.1.2	Operating mode	I_{CC_OM}	–	–	20	mA	I_{out} = 4 A on two outputs
6.1.3	Operating mode and reverse output current	$I_{CC\_OM\_REV}$	–	–	20	mA	I_{outp} = -1 A on one output, I_{out} = 4 A on two other outputs

6.2 Inputs

Electrical Characteristics: Inputs (NONx, PChx, NRESx, NCS, CLK, SDI, HS_Diag)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.2.1	Low level	V_{INL}	-0.3	–	0.2 × V_{CC}	V	–
High Level							
6.2.2	All inputs except HS_Diag	V_{INH}	0.7 × V_{CC}	–	V_{CC} + 0.3	V	–
6.2.3	HS_Diag	V_{HS_DiagH}	0.3 × V_{CC}	–	7	V	–
Hysteresis							
6.2.4	NONx, Pchx, NRESx	V_{HYST}	0.85	–	–	V	–
6.2.5	NCS, CLK, SDI	V_{HYST_SPI}	0.2	–	–	V	–
Input Current							
6.2.6	All inputs except HS_Diag pull-up current	I_{IN}	-100	–	-20	µA	0 < V_{IN} < 0.9 V_{CC}
6.2.7	HS_Diag pull-down current	I_{IN}	20	–	100	µA	500 mV < V_{IN} < V_{CC}
6.2.8	ΔI_{IN} during reverse output current	I_{IN}	-200	–	200	µA	I_{outp} = -1 A on one output

6.3 Outputs

Electrical Characteristics: Serial Data Output (SDO)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.1	High output level	V_{SDOH}	V_{CC} - 0.4	–	–	V	I_{SDO} = -2 mA
6.3.2	Low output level	V_{SDOL}	–	–	0.4	V	I_{SDO} = 3.2 mA
6.3.3	Tristate leakage current	I_{SDOL}	-10	–	10	µA	NCS = HIGH; V_{SDO} = 0 … V_{CC}

Electrical Characteristics: Control HS Outputs (NCTLx)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.4	High output level	V_{NCTLH}	V_{CC} - 1	–	–	V	I_{NCTL} = -10 mA
6.3.5	Low output level	V_{NCTLL}	–	–	0.1	V	I_{NCTL} = 1 mA
6.3.6	Peak current at L → H transition	$I_{P\_NCTL\_LH}$	–	–	-35	mA	V_{NCTL} = V_{CC} - 4 V
6.3.7	Peak current at H → L transition	$I_{P\_NCTL\_HL}$	40	–	–	mA	V_{NCTL} = 4 V

Electrical Characteristics: Power Outputs (OUTx)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.8	ON resistance at V_{CC} = 5 V	R_{DSON1}	–	–	300	mΩ	1) I_{out} = 5 A; V_{CC} = 5 V; T_j = 150 °C
6.3.9	Clamp voltage	V_{CLP1}	80	87	94	V	1) I_{OUT} = 4 A
6.3.10	Clamp voltage at -1 A on neighbor output	V_{CLPR}	–	–	94	V	test current 100 mA
6.3.11	Matching clamp voltage	V_{CLPM}	V_{CLP} - 7	–	V_{CLP} + 7	V	–
6.3.12	Leakage current	I_{OUTL}	–	–	10	µA	V_{OUT} = 18 V
6.3.13	Neg. output voltage ramp (75% × V_{bat} … 25% × V_{bat}, inductive load)	O_{VRn}	–	20	100	V/µs	see **Chapter 7.2** 1)2)
6.3.14	Pos. output voltage ramp (25% × V_{bat} … 70 V, inductive load)	O_{VRp}	–	100	200	V/µs	see **Chapter 7.2** 1)2)3)

Electrical Characteristics: Power Outputs (OUTx) (cont'd)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.15	Turn ON delay (NON 50%; V_{out} = 25% × V_{bat} inductive load)	td_{ON}			1.5	µs	see **Chapter 7.2** 1)2)
6.3.16	Turn OFF delay (NON 50%; V_{out} = 70 V, inductive load)	td_{OFF}			1.5	µs	see **Chapter 7.2** 1)2)

1) Characteristics tested in different conditions than the specification and guaranteed by correlation.
2) Measured with resistive load.
3) The design is optimized for low EM emissions (no clamp overshoot).

Electrical Characteristics: Power Outputs Reverse Diode

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.3.17	Reverse voltage drop	V_{RDa}	0.8	–	1.5	V	for I_{out} = -5.0 A (200 µs pulse)
6.3.18	Reverse voltage drop	V_{RDb}	0.6	–	1.5	V	for I_{out} = -2.5 A (200 µs pulse)

6.4 Current Control

Electrical Characteristics: Current Control[1)]

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
I_P Current (with R_{IP} = 13.5 kΩ)							
6.4.1	Absolute value at -40 °C	I_{P_C}	8.5	–	13.0	A	$I_P = k_P / R_{IP}$
6.4.2	Absolute value at 25 °C and 125 °C	I_{P_RH}	10	–	13.0	A	see **Chapter 7.1**
6.4.3	Matching at -40/25 °C	I_{PX}-I_{PY_C}	-17% × I_P	–	+17% × I_P		–
6.4.4	Matching at 125 °C	I_{PX}-I_{PY_RH}	-13% × I_P	–	+13% × I_P		–
6.4.5	Matching temp drift	$\Delta(I_{PX}$-$I_{PY})$	-2% × I_P	–	+2% × I_P		2)
I_H Current (with R_{IH} = 14.8 kΩ)							
6.4.6	Absolute value at -40 °C	I_{H_C}	1.4	–	2.6	A	$I_H = k_H / R_{IH}$
6.4.7	Absolute value at 25 °C and 125 °C	I_{H_RH}	1.8	–	2.8	A	see **Chapter 7.1**
6.4.8	Static hysteresis	ΔI_{H2}	7% × I_H	–	17% × I_H		–
6.4.9	Matching at -40/25 °C	I_{HX}-I_{HY_C}	-17% × I_H	–	+17% × I_H		–
6.4.10	Matching at 125 °C	I_{HX}-I_{HY_RH}	-13% × I_H	–	+13% × I_H		–
6.4.11	Matching temp drift	$\Delta(I_{HX}$-$I_{HY})$	-4% × I_H	–	+4% × I_H		2)
I_{PC} Current (with R_{IPC} = 17.4 kΩ)							
6.4.12	Absolute value at -40 °C	I_{PC_C}	0.6	–	1.25	A	$I_{PC} = k_{PC} / R_{IPC}$
6.4.13	Absolute value at 25 °C and 125 °C	I_{PC_RH}	0.7	–	1.25	A	see **Chapter 7.1**
6.4.14	Static hysteresis	ΔI_{PC2}	7% × I_{PC}	12.5% × I_{PC}	15% × I_{PC}		–
6.4.15	Matching at -40/25 °C	I_{PCX}-I_{PCY_C}	-17% × I_{PC}	–	+17% × I_{PC}		–
6.4.16	Matching at 125 °C	I_{PCX}-I_{PCY_RH}	-13% × I_{PC}	–	+13% × I_{PC}		–
6.4.17	Matching temp drift	$\Delta(I_{PCX}$-$I_{PCY})$	-4% × I_{PC}	–	+4% × I_{PC}		2)

1) No reverse current on any outputs are allowed. External measures against reverse current must be applied.

2) Parameter specified by design, not subject to production test.

6.5 Current Control Timings

Electrical Characteristics: Current Control Timings (Load capacitor at NCTLx = 100 pF)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
NCTL2 Current Control Delay							
6.5.1	delay from Pch14 50% × V_{CC} to NCTL2 50% × V_{CC}	td_{NCTL2a}	–	–	200	ns	–
6.5.2	delay from HS_diag 50% × V_{CC} to NCTL2 50% × V_{CC}	td_{NCTL2c}	–	–	500	ns	–
NCTL3 Current Control Delay							
6.5.3	delay from HS_diag 50% × V_{CC} to NCTL3 50% × V_{CC}	td_{NCTL3c}	–	–	500	ns	–

6.6 Diagnostic and Protections

Electrical Characteristics: Diagnostic and Protections

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.6.1	Overcurrent threshold	I_{OFF}	1.18 × I_P	1.4 × I_P	1.62 × I_P	A	1)
6.6.2	Overtemperature threshold	T_{OFF}	155	–	185	°C	2)3)
6.6.3	HS diag input: filter and setup time	t_{HS}	50	–	250	ns	–
6.6.4	Overcurrent / Overtemperature Shutdown filter and delay time	t_{OFF}	8	–	18	µs	1)
6.6.5	Pull-up resistor	$R_{PULL-UP}$	40	–	150	kΩ	–
6.6.6	OFF state overvoltage threshold	V_{OL}	0.6 × V_{CC}	–	0.7 × V_{CC}	V	–
6.6.7	OFF state overvoltage filter and delay time	t_{OL}	3.5	–	4.5	ms	–
6.6.8	Peak current overtime threshold	t_{Pmax}	–	t_1	–	µs	–
6.6.9	Peak current undertime threshold	t_{Pmin}	10	–	60	µs	–
6.6.10	V_{CC} undervoltage	V_{CCRES}	3.35	–	3.95	V	–
6.6.11	Undervoltage protection Max ON-time after a output voltage ramp from: 0 V to 25 V at V_{CC} = 0 V to 5.5 V	t_{rpON}	–	–	100	µs	–

1) Not subject to production test, specified by design.
2) Characteristics tested at wafer level only (with special testpads), not on packaged parts.
3) Characteristics tested in different conditions than the specification and guaranteed by correlation.

6.7 SPI Timings

Electrical Characteristics: SPI Timings (see **Figure 17**), Load capacitor at SDO = 100 pF

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.7.1	Clock frequency (50% duty cycle)	f_{CLK}	–	–	3	MHz	–
6.7.2	Minimum time CLK = HIGH	t_{CLH}	100	–	–	ns	–
6.7.3	Minimum time CLK = LOW	t_{CLL}	100	–	–	ns	–
6.7.4	Propagation delay CLK to data at SDO valid	t_{PCLD}	–	–	100	ns	1)
6.7.5	NCS = LOW to data at SDO valid	t_{CSDV}	–	–	100	ns	1)
6.7.6	CLK low before NCS low (setup time CLK to NCS change H/L)	t_{SCLCH}	100	–	–	ns	–
6.7.7	CLK change L/H after NCS = low	t_{HCLCL}	100	–	–	ns	–
6.7.8	SDI input setup time (CLK change H/L after SDI data valid)	t_{SCLD}	20	–	–	ns	–
6.7.9	SDI input hold time (SDI data hold after CLK change H/L)	t_{HCLD}	20	–	–	ns	–
6.7.10	CLK low before NCS high	t_{SCLCL}	150	–	–	ns	–
6.7.11	CLK high after NCS high	t_{HCLCH}	150	–	–	ns	–
6.7.12	NCS L/H to output data float	t_{PCHDZ}	–	–	100	ns	1)
6.7.13	Capacitance at SDI, SDO, CLK, NCS	C_x	–	–	15	pF	1) Ceramic Capacitor
6.7.14	NCS filter time (pulses ≤ t_{fNCS} will be ignored)	t_{fNCS}	10	–	40	ns	1)

1) Not subject to production test, specified by design

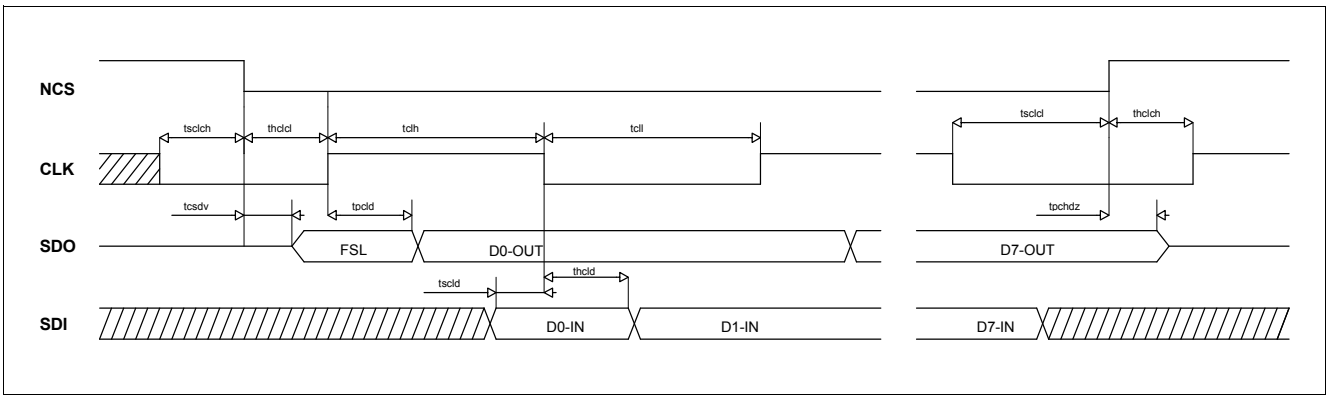


Figure 17 SPI Timings

Electrical Characteristics: Internal Clock

(see SMD ceramic resonator specification n° S108 058 007 / 65 92 36.20.89, **Figure 18**)

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.7.15	External resonator frequency	f_{OSC}	–	8	–	MHz	–
6.7.16	Internal frequency tolerance	Δf_{OSC}	-3%	–	+3%	f_{OSC}	–

Electrical Characteristics: Programmable Timings

V_{CC} = 4.5 V to 5.5 V, T_{CASE} = -40 ·C to +125 ·C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
t_1 Time							
6.7.17	Number of coding bit via SPI		–	3	–		–
6.7.18	t_1 default value	t1_0	–	192	–	µs	(0, 0, 0)
6.7.19	t_1 LSB (Least Significant Bit)	t1_lsb	–	32	–	µs	–
6.7.20	t_1 max value	t1_max	–	416	–	µs	(1, 1, 1)
t_2 Time							
6.7.21	Number of coding bit via SPI		–	5	–		–
6.7.22	t_2 default value	t2_0	–	0	–	µs	(0, 0, 0, 0, 0)
6.7.23	t_2 LSB (Least Significant Bit)	t2_lsb	–	2	–	µs	–
6.7.24	t_2 max value	t2_max	–	62	–	µs	(1, 1, 1, 1, 1)

Attention: To avoid any unknown logic state, t_1 and t_2 values must be latched at the end of t_2 time. Moreover, one latch is needed for each group (A and B) for overlapping reasons. At last, as t_1 and t_2 can be whenever changed, t_1 and t_2 should be stored in TLE6270R to release the SPI bus prior to being taken into account by the internal counters.

Resonator

Electrical Characteristics

Nominal Oscillating Frequency	8.000MHz
Oscillating Frequency Tolerance	+/-0.5%
Built-in Capacitance value	30pF +/-20%
Resonant Impedance	
Maximum Resonant Impedance	40Ohm max.
Variation by Temperature Change	10Ohm max. at 170°C, 6sec.
Insulation Resistance	500MOhm min (at 10VDC)
Withstanding Voltage	100VDC, 5 sec. max.
Absolute Maximum Voltage	
Maximum DC Voltage	6VDC
Maximum Input Voltage	15Vpp
Temperature Characteristic (-40 to +125°C)	+/-0.4% max.
Operating Temperature Range	-40 to +125°C
Storage Temperature Range	-55 to +125°C

Application Diagram

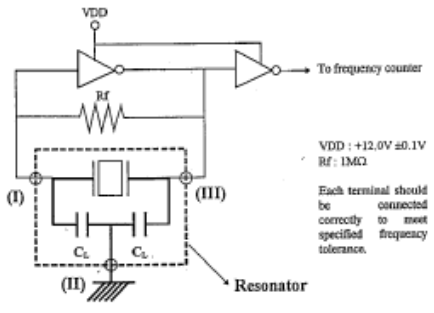


Figure 18 Application Hint: Example of Resonator

7 Diagrams

7.1 Typical Laws

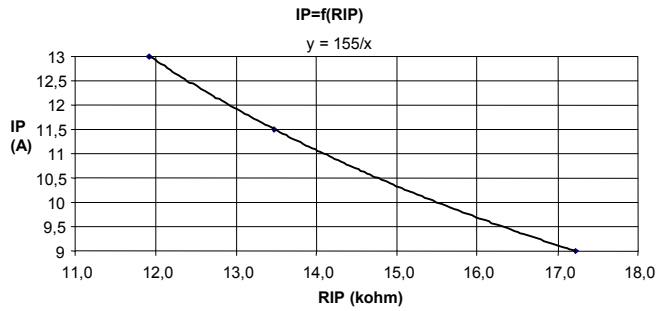


Figure 19 $I_P(R_{IP})$ (temp = 25 °C)

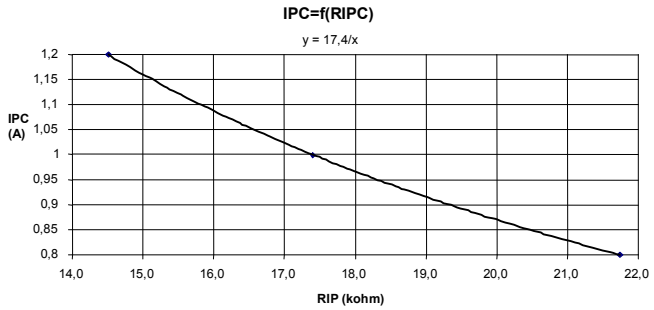


Figure 20 $I_{PC}(R_{IPC})$ (temp = 25 °C)

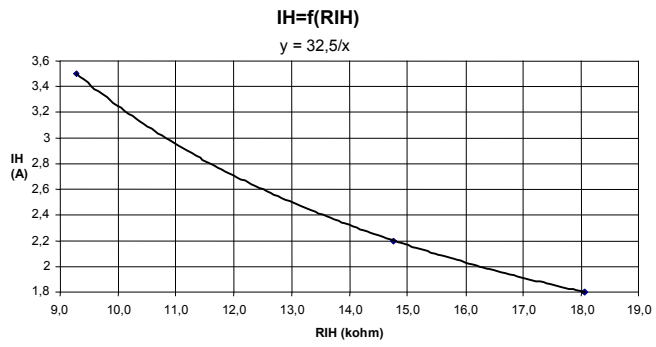


Figure 21 $I_H(R_{IH})$ (temp = 25 °C)

7.2 Output Timings Diagram

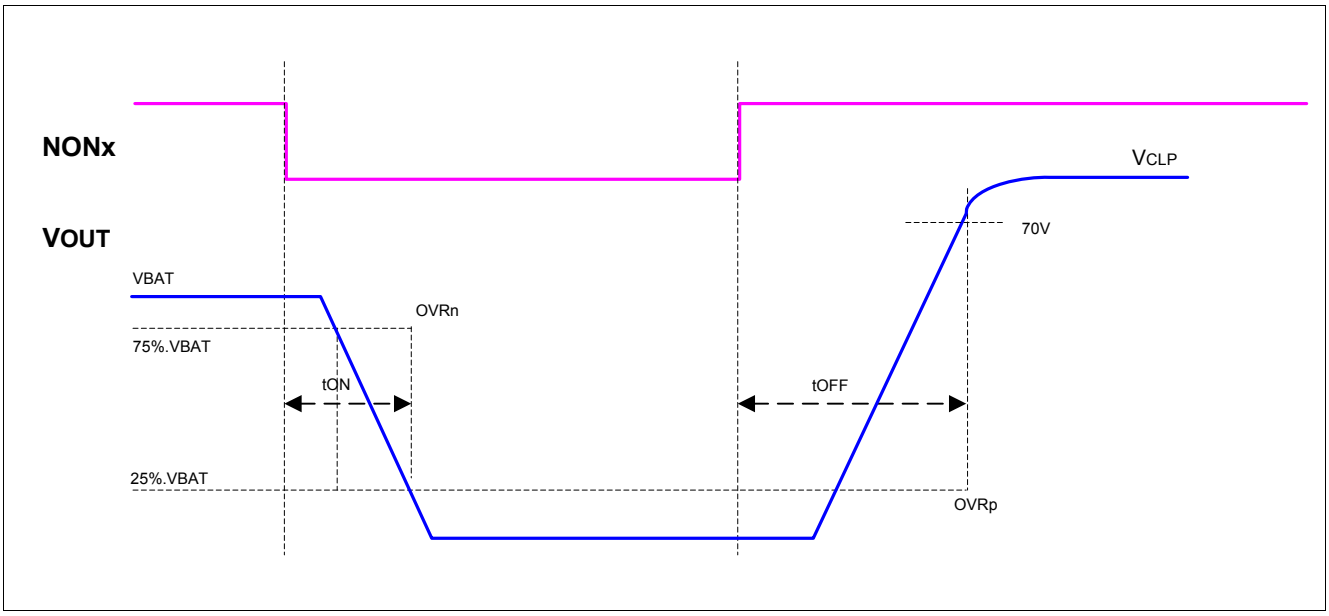


Figure 22 Output Timing

8 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Principle Diagram of Injection System

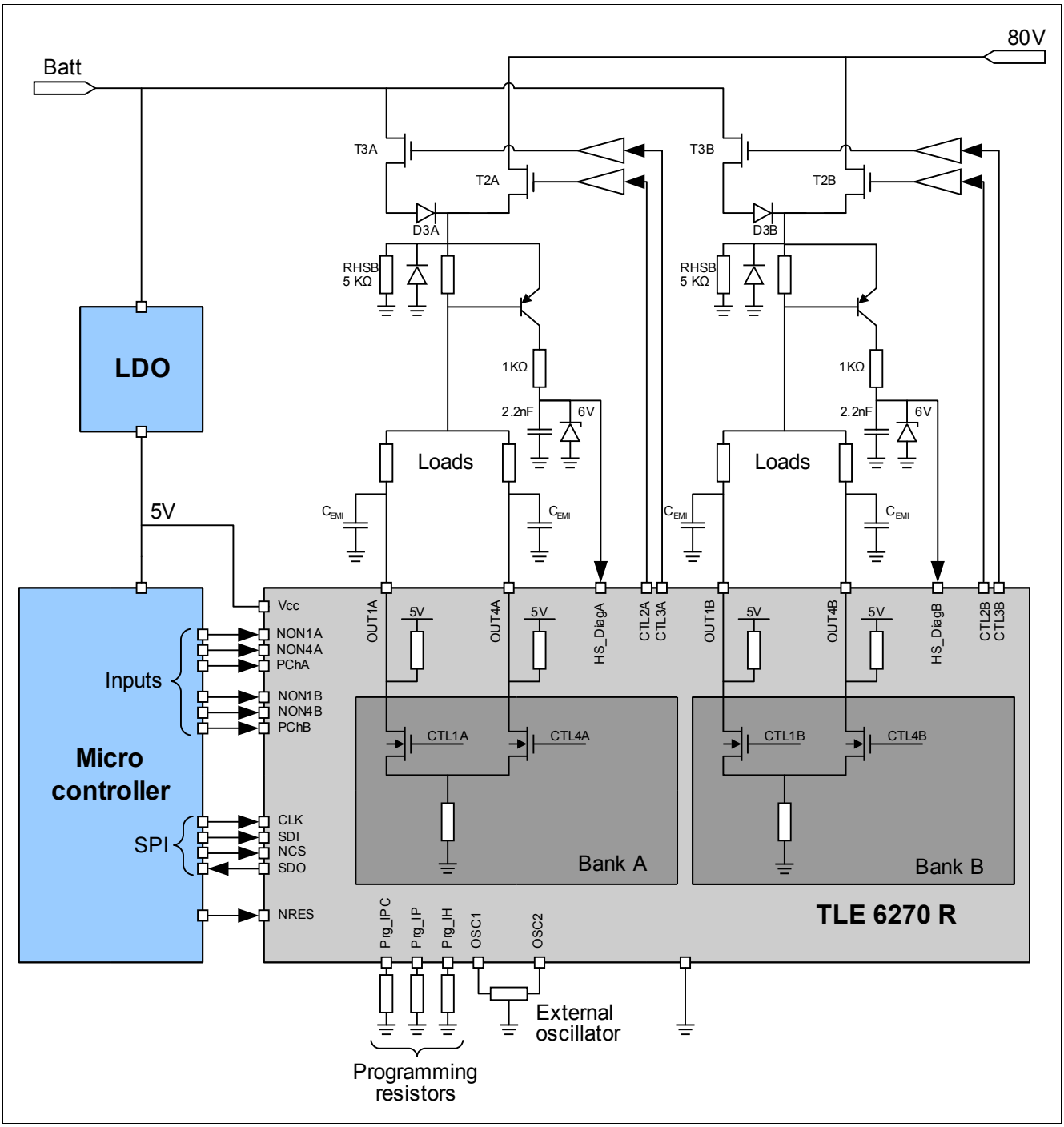


Figure 23 Application Diagram

Note: All values mentioned are typical values.

Note: In order to program different t1 and t2 times the resonator frequency could be adjusted

8.2 Typical Waveform Diagrams for One and Two Outputs Control

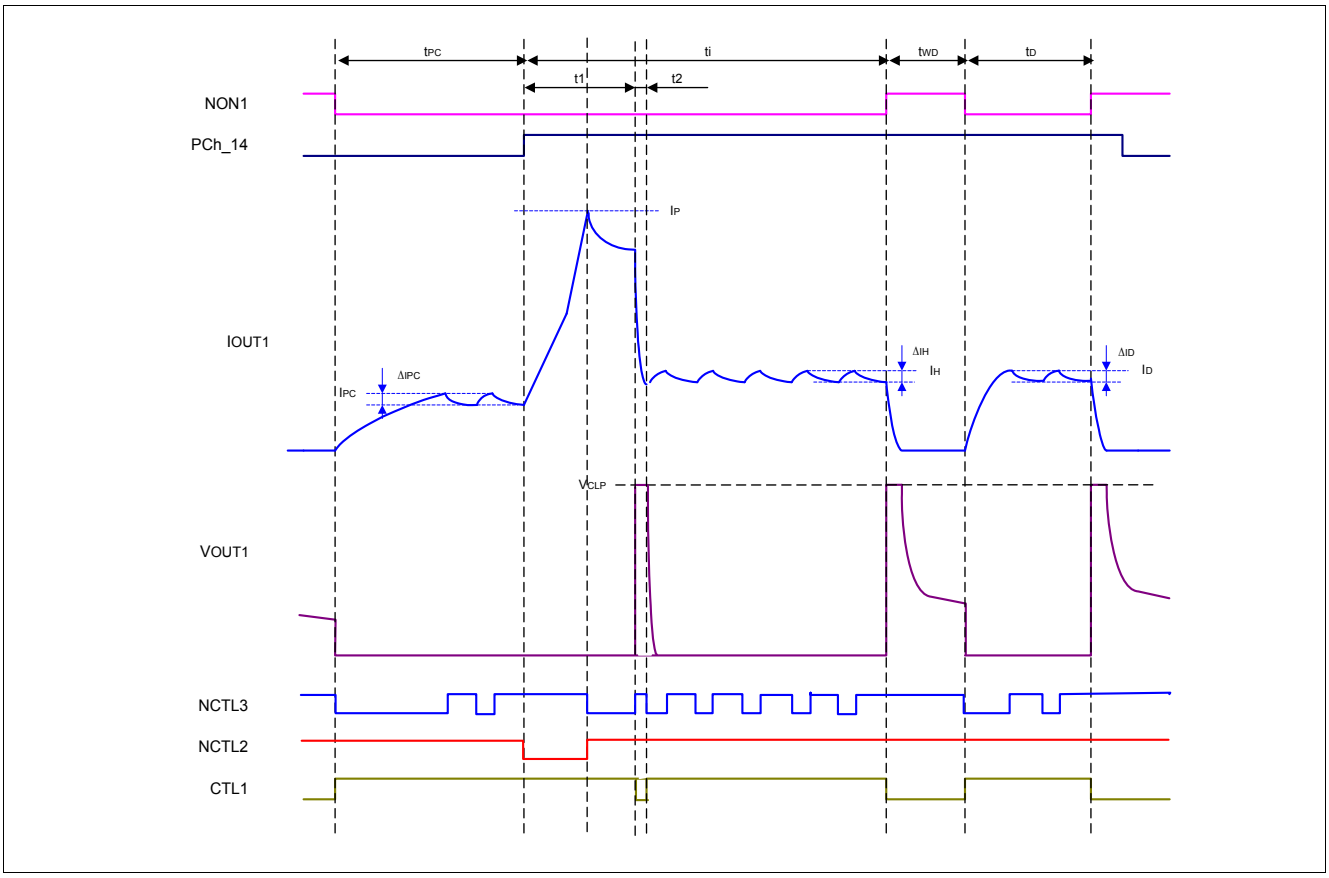


Figure 24 Waveform Diagram for One Output Control

- t_{pc} is typically 1 ms. It can be set to 100 ns minimum.
- t_{wd} is typically 200 µs.
- t_d is typically 150 µs.

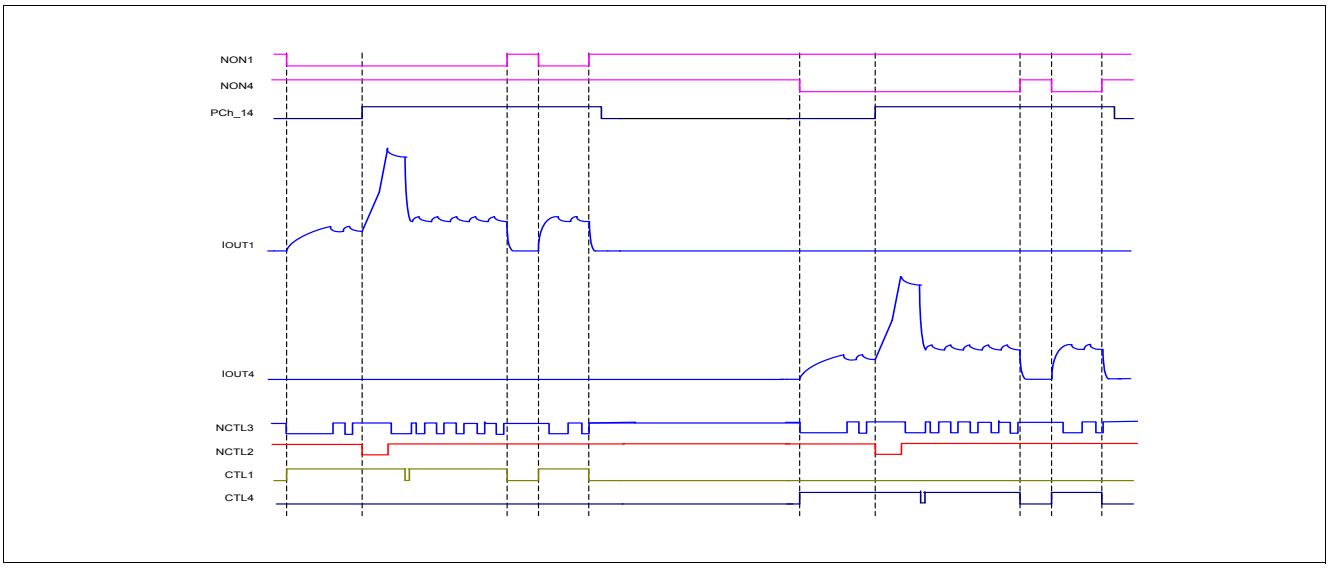


Figure 25 Waveform Diagram for Two Outputs Control

Note: For each group (A or B), there is no overlapping between the channels 1 and 4.

9 Package Outlines

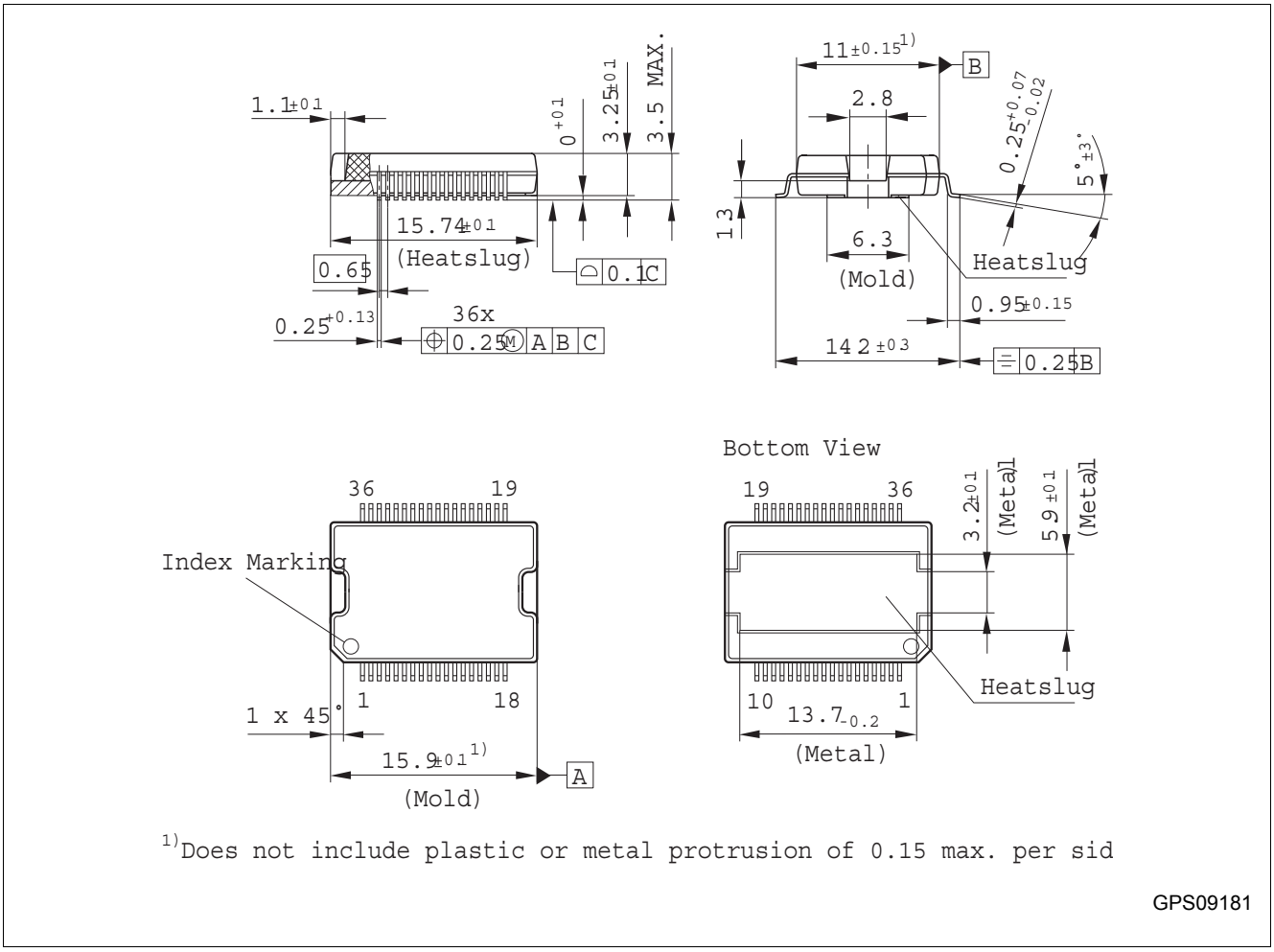


Figure 26 P-DSO-36 (Plastic Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

10 Revision History

Revision	Date	Changes
1.3.1	2011-06-27	Cover updated according to new template **Figure 1**: edited **Figure 23**: edited, changed D3A, D3B placement
1.3	2008-10-22	Updated data sheet to newest template revision **Figure 1**: changed **Chapter 5.2**: added details **Chapter 5.4.1**: added paragraph regarding open load detection **Table 2**: modified **Table 3**: modified **Figure 15**: modified **Table 4**: modified **Chapter 8**: application information chapter moved **Figure 23**: changed and second note added All pages: editorial changes
1.1	2008-08-25	Initial version of RoHS-compliant derivate of TLE6270R Datasheet converted to green

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