General Description

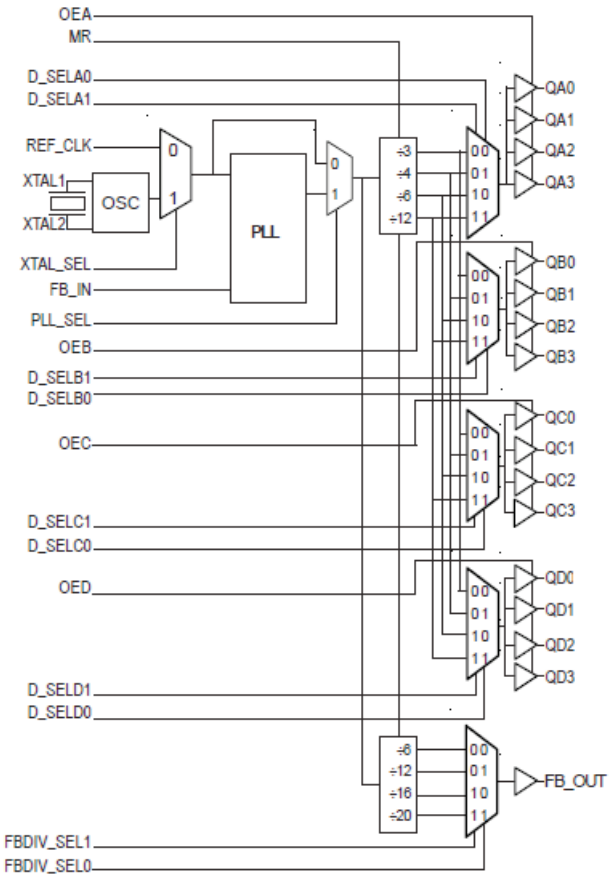
The 8761I is a low voltage, low skew PCI / PCI-X clock generator . The 8761I has a selectable REF_CLK or crystal input. The REF_CLK input accepts LVCMOS or LVTTL input levels. The 8761I has a fully integrated PLL along with frequency configurable clock and feedback outputs for multiplying and regenerating clocks with “zero delay”. Using a 20MHz or 25MHz crystal or a 33.333MHz or 66.666MHz reference frequency, the 8761I will generate output frequencies of 33.333MHz, 66.666MHz, 100MHz and 133.333MHz simultaneously.

The low impedance LVCMOS/LVTTL outputs of the 8761I are designed to drive 50Ω series or parallel terminated transmission lines.

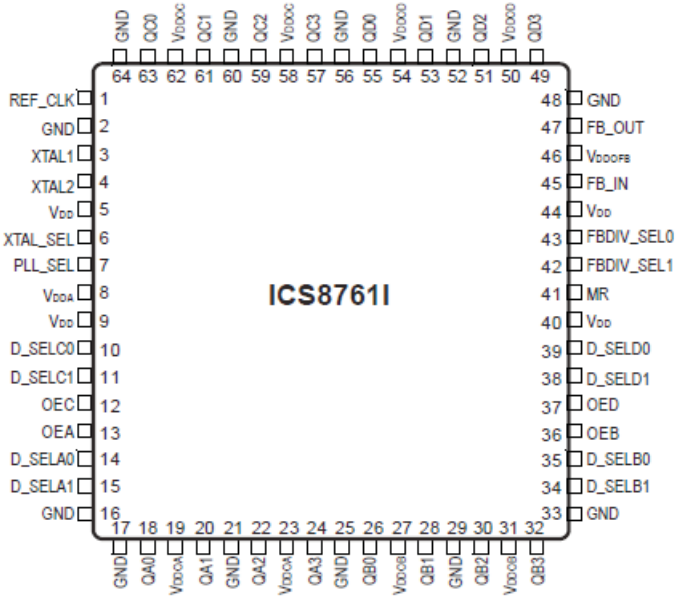
Features

- Fully integrated PLL
- Seventeen LVCMOS/LVTTL outputs, 15Ω typical output impedance
- Selectable crystal oscillator interface or LVCMOS/LVTTL REF_CLK
- Maximum output frequency: 166.67MHz
- Maximum crystal input frequency: 40MHz
- Maximum REF_CLK input frequency: 83.33MHz
- Individual banks with selectable output dividers for generating 33.333MHz, 66.66MHz, 100MHz and 133.333MHz simultaneously
- Separate feedback control for generating PCI / PCI-X frequencies from a 20MHz or 25MHz crystal or 33.333MHz or 66.666MHz reference frequency
- Cycle-to-cycle jitter: 70ps (maximum)
- Period jitter, RMS: 17ps (maximum)
- Output skew: 250ps (maximum)
- Bank skew: 50ps (maximum)
- Static phase offset: 0 ± 150ps (maximum)
- Full 3.3V or 3.3V core, 2.5V multiple output supply modes
- -40°C to 85°C ambient operating temperature
- Available in both standard and lead-free RoHS-compliant packages

Block Diagram



Pin Assignment



64-Lead LQFP
10mm x 10mm x 1.4mm package body
Y package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	REF_CLK	Input	Pulldown	Reference clock input. LVCMOS / LVTTL interface levels.
2, 16, 17, 21, 25, 29, 33, 48, 52, 56, 60, 64	GND	Power		Power supply ground.
3, 4	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
5, 9, 40, 44	V_{DD}	Power		Core supply pins.
6	XTAL_SEL	Input	Pullup	Selects between crystal oscillator or reference clock as the PLL reference source. Selects XTAL inputs when HIGH. Selects REF_CLK when LOW. LVCMOS / LVTTL interface levels.
7	PLL_SEL	Input	Pullup	Selects between PLL and bypass mode. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTL interface levels.
8	V_{DDA}	Power		Analog supply pin. See Applications Note for filtering.
10, 11	D_SELC0, D_SELC1	Input	Pulldown	Selects divide value for Bank C outputs as described in Table 3. LVCMOS / LVTTL interface levels.
12	OEC	Input	Pullup	Determines state of Bank C outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
13	OEA	Input	Pullup	Determines state of Bank A outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
14, 15	D_SELA0, D_SELA1	Input	Pulldown	Selects divider value for Bank A outputs as described in Table 3. LVCMOS / LVTTL interface levels.
18, 20, 22, 24	QA0, QA1, QA2, QA3	Output		Bank A clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
19, 23	V_{DDOA}	Power		Output supply pins for Bank A outputs.
26, 28, 30, 32	QB0, QB1, QB2, QB3	Output		Bank B clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
27, 31	V_{DDOB}	Power		Output supply pins for Bank B outputs.
34, 35	D_SELB1, D_SELB0	Input	Pulldown	Selects divider value for Bank B outputs as described in Table 3. LVCMOS / LVTTL interface levels.
36	OEB	Input	Pullup	Determines state of Bank B outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
37	OED	Input	Pullup	Determines state of Bank D outputs. When HIGH, outputs are enabled. When LOW, outputs are disabled. LVCMOS / LVTTL interface levels.
38, 39	D_SELD1, D_SELD0	Input	Pulldown	Selects divider value for Bank D outputs as described in Table 3. LVCMOS / LVTTL interface levels.
41	MR	Input	Pulldown	Active HIGH Master reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.
42	FBDIV_SEL1	Input	Pulldown	Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
43	FBDIV_SEL0	Input	Pullup	Selects divider value for bank feedback output as described in Table 3. LVCMOS / LVTTL interface levels.
45	FB_IN	Input	Pulldown	Feedback input to phase detector for generating clocks with “zero delay”. LVCMOS / LVTTL interface levels.

Number	Name	Type		Description
46	V_{DDOFB}	Power		Output supply pin for FB_Out output.
47	FB_OUT	Output		Feedback output. Connect to FB_IN. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
49, 51, 53, 55	QD3, QD2, QD1, QD0	Output		Bank D clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
50, 54	V_{DDOD}	Power		Output supply pins for Bank D outputs.
57, 59, 61, 63	QC3, QC2, QC1, QC0	Output		Bank C clock outputs. 15Ω typical output impedance. LVCMOS / LVTTL interface levels.
58, 62	V_{DDOC}	Power		Output supply pins for Bank C outputs.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor				51	kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				51	kΩ
C_{PD}	Power Dissipation Capacitance (per output); NOTE 1	V_{DD}, V_{DDA} = 3.465V; V_{DDOx} = 3.465V			9	pF
		V_{DD}, V_{DDA} = 3.465V; V_{DDOx} = 2.625V			11	pF
R_{OUT}	Output Impedance			15		Ω

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, V_{DDOFB}.

Table 3A. Output Control Pin Function Table

Inputs					Outputs			
MR	OEA	OEB	OEC	OED	QA0:QA3	QB0:QB3	QC0:QC3	QD0:QD3
1	1	1	1	1	LOW	LOW	LOW	LOW
0	1	1	1	1	Active	Active	Active	Active
X	0	0	0	0	HiZ	HiZ	HiZ	HiZ

Table 3B. Operating Mode Function Table

Inputs	Operating Mode
PLL_SEL	
0	Bypass
1	PLL

Table 3C. PLL Input Function Table

Inputs	
XTAL_SEL	PLL Input
0	REF_CLK
1	XTAL Oscillator

TABLE 3D. CONTROL FUNCTION TABLE

Inputs					Outputs		
					PLL_SEL =1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency Range (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	41.6 - 83.33	x 2	83.33 - 166.67	41.6 - 83.33
0	0	0	1	20.83 - 41.67	x 4	83.33 - 166.67	20.83 - 41.67
0	0	1	0	15.62 - 31.25	x 5.33	83.33 - 166.67	15.62 - 31.25
0	0	1	1	12.5 - 25	x 6.67	83.33 - 166.67	12.5 - 25
0	1	0	0	41.6 - 83.33	x 1.5	62.4 - 125	41.6 - 83.33
0	1	0	1	20.83 - 41.67	x 3	62.4 - 125	20.83 - 41.67
0	1	1	0	15.62 - 31.25	x 4	62.4 - 125	15.62 - 31.25
0	1	1	1	12.5 - 25	x 5	62.4 - 125	12.5 - 25
1	0	0	0	41.6 - 83.33	x 1	41.6 - 83.33	41.6 - 83.33
1	0	0	1	20.83 - 41.67	x 2	41.6 - 83.33	20.83 - 41.67
1	0	1	0	15.62 - 31.25	x 2.67	41.6 - 83.33	15.62 - 31.25
1	0	1	1	12.5 - 25	x 3.33	41.6 - 83.33	12.5 - 25
1	1	0	0	41.6 - 83.33	÷ 2	20.8 - 41.67	41.6 - 83.33
1	1	0	1	20.83 - 41.67	÷ 1	20.8 - 41.67	20.83 - 41.67
1	1	1	0	15.62 - 31.25	x 1.33	20.8 - 41.67	15.62 - 31.25
1	1	1	1	12.5 - 25	x 1.67	20.8 - 41.67	12.5 - 25

NOTE: D_SELX1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1. D_SELX0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

TABLE 3E. CONTROL FUNCTION TABLE (PCI CONFIGURATION)

Inputs					Outputs		
					PLL_SEL = 1	Frequency	
D_SELx1	D_SELx0	FBDIV_SEL1	FBDIV_SEL0	Reference Frequency (MHz)	QX0:QX3	QX0:QX3 (MHz)	FB_OUT (MHz)
0	0	0	0	66.67	x 2	133	66.67
0	0	0	1	33.33	x 4	133	33.33
0	0	1	0	25	x 5.33	133	25
0	0	1	1	20	x 6.67	133	20
0	1	0	0	66.67	x 1.5	100	66.67
0	1	0	1	33.33	x 3	100	33.33
0	1	1	0	25	x 4	100	25
0	1	1	1	20	x 5	100	20
1	0	0	0	66.67	x 1	66.67	66.67
1	0	0	1	33.33	x 2	66.67	33.33
1	0	1	0	25	x 2.67	66.67	25
1	0	1	1	20	x 3.33	66.67	20
1	1	0	0	66.67	÷ 2	33.33	66.67
1	1	0	1	33.33	÷ 1	33.33	33.33
1	1	1	0	25	x 1.33	33.33	25
1	1	1	1	20	x 1.67	33.33	20

NOTE: D_SELx1 denotes D_SELA1, D_SELB1, D_SELC1, and D_SELD1. D_SELx0 denotes D_SELA0, D_SELB0, D_SELC0, and D_SELD0. QX0:QX3 denotes QA0:QA3, QB0:QB3, QC0:QC3, and QD0:QD3.

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDOx} + 0.5V
Package Thermal Impedance, θ_{JA}	41.1°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDA} = V_{DDOX}$ = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDOx}	Output Supply Voltage; NOTE 1		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				175	mA
I_{DDA}	Analog Supply Current				55	mA
I_{DDOx}	Output Supply Current; NOTE 2				25	mA

NOTE 1: V_{DDOx} denotes V_{DDOA}, V_{DDOB}, V_{DDOC}, V_{DDOD}, and V_{DDOFB}.
NOTE 2: I_{DDOx} denotes I_{DDOA}, I_{DDOB}, I_{DDOC}, I_{DDOD}, and I_{DDOFB}.

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDA} = 3.3V±5\%$, $V_{DDOX} = 3.3V±5\%$ or $2.5V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	OEA:OED, XTAL_SEL, MR, D_SELAx, D_SELBx, FB_IN, D_SELCx, D_SELDx, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		2		V_{DD} + 0.3	V
		REF_CLK		2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	OEA:OED, XTAL_SEL, MR, D_SELAx, D_SELBx, FB_IN, D_SELCx, D_SELDx, PLL_SEL, FBDIV_SEL0, FBDIV_SEL1		-0.3		0.8	V
		REF_CLK		-0.3		1.3	V
I_{IH}	Input High Current	D_SELAx, D_SELBx, FB_IN, MR, D_SELCx, D_SELDx, REF_CLK, FBDIV_SEL1	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			150	µA
		XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED	$V_{DD} = V_{IN}$ = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	D_SELAx, D_SELBx, FB_IN, MR, D_SELCx, D_SELDx, REF_CLK, FBDIV_SEL1	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-5			µA
		XTAL_SEL, PLL_SEL, FBDIV_SEL0, OEA:OED	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA
V_{OH}	Output High Voltage; NOTE 1		V_{DDOx} = 3.465V	2.6			V
			V_{DDOx} = 2.625V	1.8			
V_{OL}	Output Low Voltage; NOTE 1		V_{DDOx} = 3.465V or 2.625V			0.5	V
I_{OZL}	Output Tristate Current Low			-5			µA
I_{OZH}	Output Tristate Current High					5	µA

NOTE 1: Outputs terminated with 50Ω to $V_{DDOx}/2$. See Parameter Measurement Information section, "Output Load Test Circuit".

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		38	MHz
Equivalent Series Resistance (ESR)				70	Ω
Shunt Capacitance			7		pF
Drive Level				1	mW

Table 6. PLL Input Reference Characteristics, $V_{DD} = V_{DDA} = V_{DDOx} = 3.3V±5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{REF}	Reference Frequency		12.5		83.33	MHz

TABLE 7A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDOX} = 3.3V \pm 5\%$, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1, 7	f = 50MHz	-150		150	ps
*t*sk(b)	Bank Skew; NOTE 2, 6				50	ps
*t*sk(o)	Output Skew; NOTE 3, 6				250	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; 6	f = 50MHz; NOTE 4, 7			70	ps
		f = 25MHz XTAL, 133.3MHz out			190	ps
*t*jit(per)	Period Jitter, RMS; NOTE 4, 6, 7, 8				17	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		800	ps
odc	Output Duty Cycle; NOTE 5, 7		45		55	%

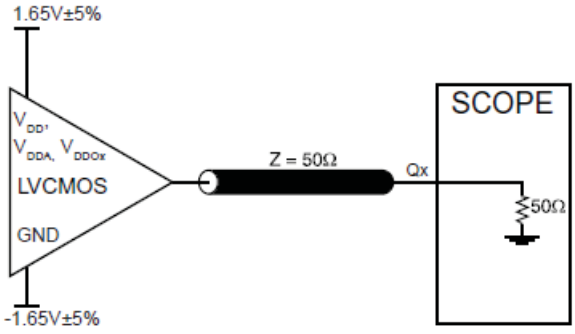
NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured from $V_{DD}/2$ of the input to $V_{DDOx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Jitter performance using LVCMOS inputs.
NOTE 5: Measured using REF_CLK. For XTAL input, refer to Application Note.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: Tested with D_SELXX =10 (divide by 6); FBDIV_SEL = 00 (divide by 6).
NOTE 8: This parameter is defined as an RMS value.

TABLE 7B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDOx} = 2.5V \pm 5\%$, T_A = -40°C TO 85°C

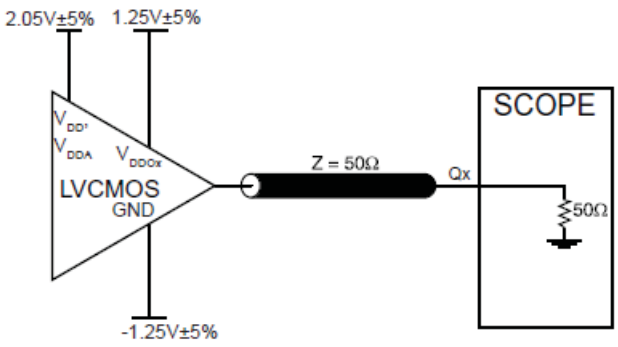
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				166.67	MHz
t(Ø)	Static Phase Offset; NOTE 1, 7	f = 50MHz	-350		20	ps
*t*sk(b)	Bank Skew; NOTE 2, 6				50	ps
*t*sk(o)	Output Skew; NOTE 3, 6				250	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 6	f = 50MHz; NOTE 4, 7			70	ps
		f = 25MHz XTAL, 133.3MHz out			190	ps
*t*jit(per)	Period Jitter, RMS; NOTE 4, 6, 7, 8				17	ps
t_L	PLL Lock Time				1	ms
t_R / t_F	Output Rise/Fall Time	20% to 80%	250		800	ps
odc	Output Duty Cycle; NOTE 5, 7		45		55	%

NOTE 1: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable. Measured from $V_{DD}/2$ of the input to $V_{DDOx}/2$ of the output.
NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDOx}/2$.
NOTE 4: Jitter performance using LVCMOS inputs.
NOTE 5: Measured using REF_CLK. For XTAL input, refer to Application Note.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 7: Tested with D_SELXX =10 (divide by 6); FBDIV_SEL = 00 (divide by 6).
NOTE 8: This parameter is defined as an RMS value

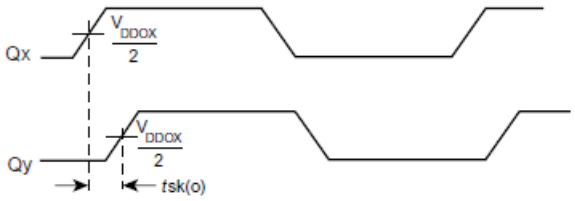
Parameter Measurement Information



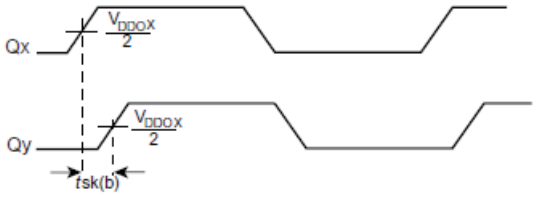
3.3V Core/3.3V Output Load AC Test Circuit



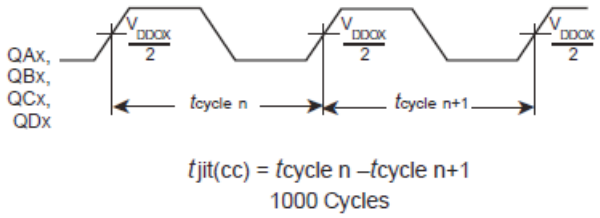
3.3V Core/2.5V Output Load AC Test Circuit



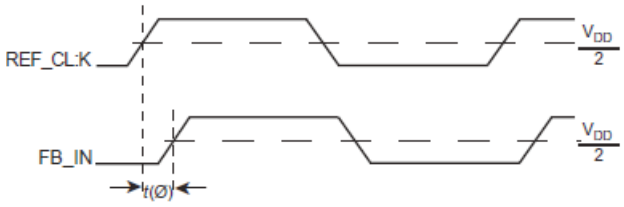
Output Skew



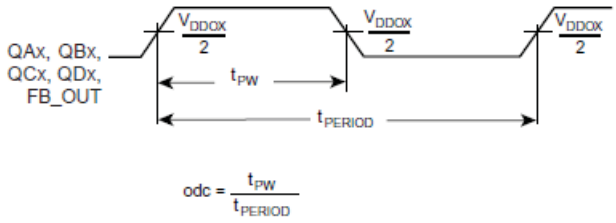
Bank Skew (Where X denotes outputs in the same Bank)



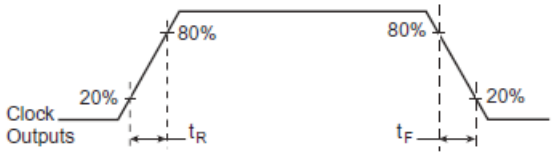
Cycle-to-Cycle Jitter



Static Phase Offset



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 8761I provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a ferrite bead along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA}.

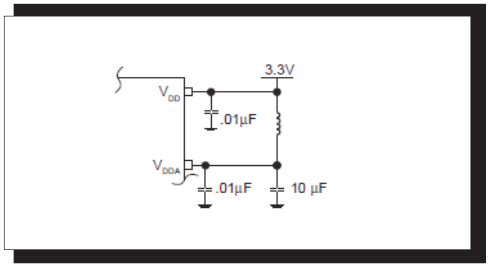


Figure 1. Power Supply Filtering

Crystal Input Interface

The 8761I crystal interface is shown in *Figure 2.* While layout the PC Board, it is recommended to provide C1 and C2 spare footprints for frequency fine tuning. For an 18pF parallel resonant crystal, the C1 and C2 are expected to be ~10pF and ~5pF respectively.

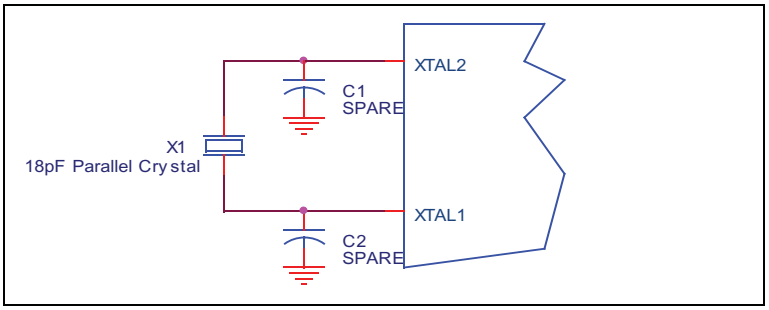


Figure 2. Crystal Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Input:
For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input:
For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Output:
All unused LVCMOS output can be left floating. We recommend that there is no trace attached.

Schematic Example

Figure 3 shows a schematic example of the 8761I. In this example, the input is driven by an 18pF parallel crystal. The decoupling capacitors should be physically located near the power pin. For 8761I, the unused clock outputs can be left floating. The optional C1 and C2 are spare footprints for frequency fine tuning.

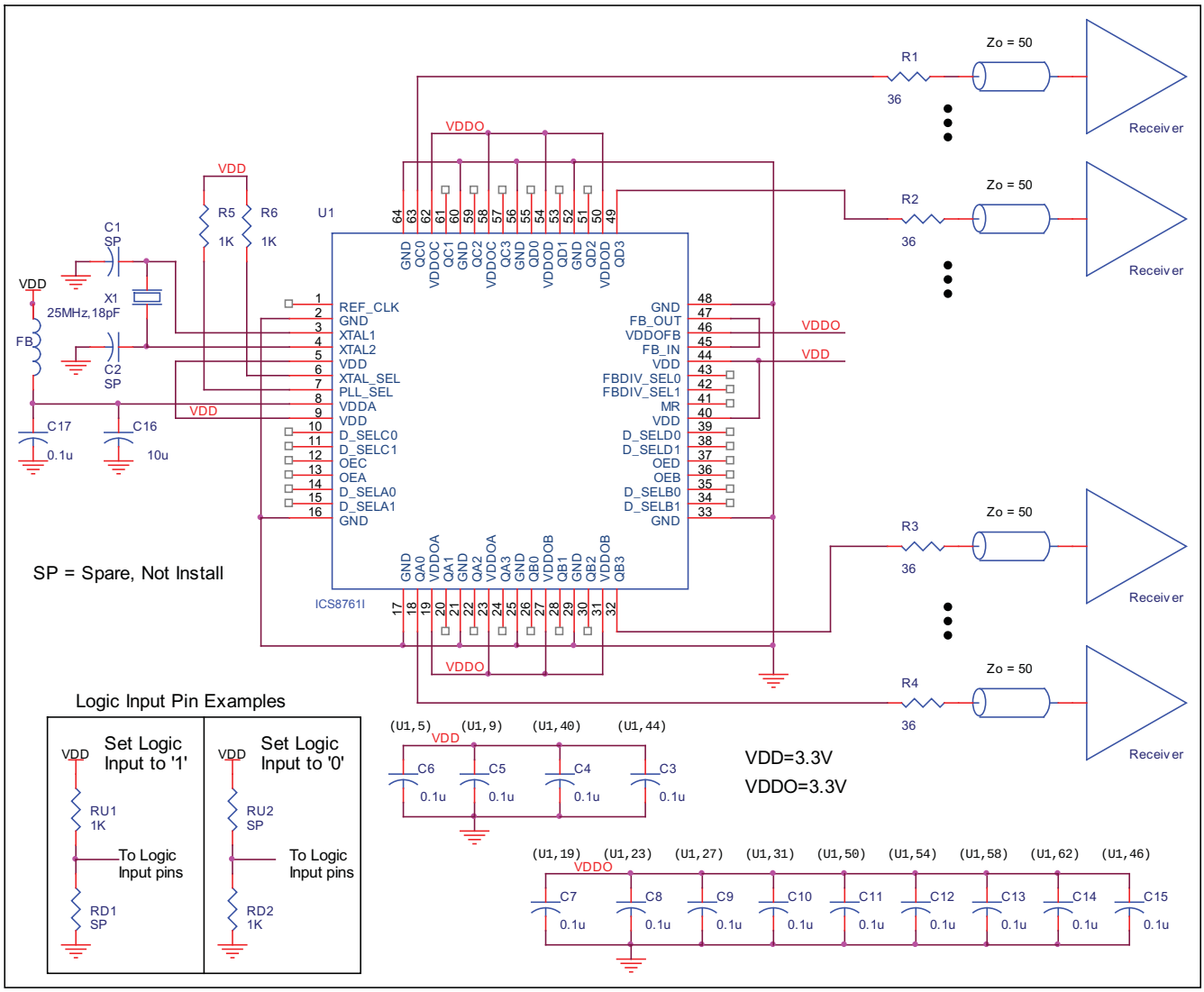


Figure 3. 8761I Clock Generator Schematic Example

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 64 Lead LQFP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	58.8°C/W	48.5°C/W	43.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	41.1°C/W	35.8°C/W	33.6°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8761I is: 6040

Package Outline - Y Suffix for 64 Lead LQFP

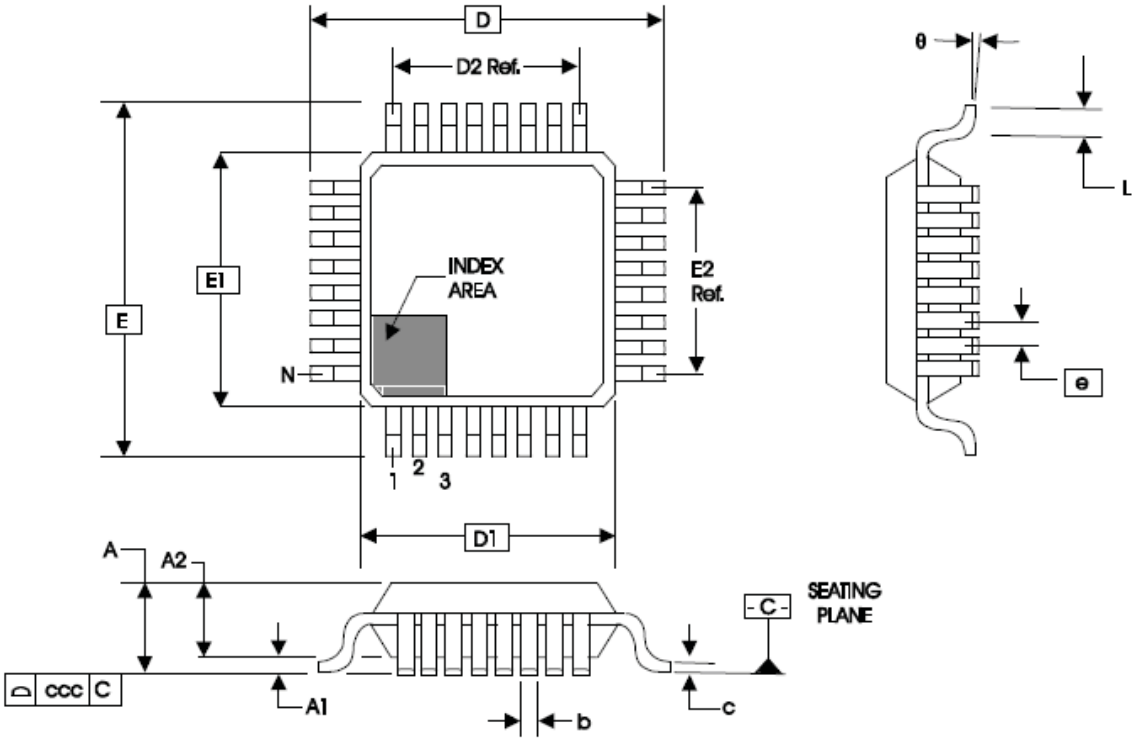


Table 9. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCD		
	MINIMUM	NOMINAL	MAXIMUM
N		64	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	--	0.27
c	0.09	--	0.20
D		12.00 BASIC	
D1		10.00 BASIC	
D2		7.50 Ref.	
E		12.00 BASIC	
E1		10.00 BASIC	
E2		7.50 Ref.	
e		0.50 BASIC	
L	0.45	--	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8761CYILF	ICS8761CYILF	64 lead “Lead Free” LQFP	Tray	-40°C to +85°C
8761CYILF	ICS8761CYILF	64 lead “Lead Free” LQFP	Tape and Reel	-40°C to +85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T10	1 9 13	Features Section - added Lead-Free bullet. Added Crystal Section. Ordering Information Table - added Lead-Free Part Number. Updated format throughout the data sheet.	10/5//04
B	T2 T5 T10	3 6 9 10 11 14	Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. Crystal Characteristics Table - added Drive Level. Power Supply Filtering Techniques - corrected last sentence in the paragraph to read “Figure 1 illustrates how a ferrite bead along...” from “Figure 1 illustrates how a 10Ω resistor along...”. Corrected Power Supply Filtering diagram. Added *Recommendations for Unused Input and Output Pins.* Corrected Schematic Example diagram. Ordering Information Table - added Lead-Free note.	1/13/06
B	T10	14 16	Updated datasheet’s header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	7/27/10
C	T10	1 14	Removed ICS from part numbers where needed. Features Section - removed reference to leaded package. Ordering Information - removed quantity from tape and reel. Deleted LF note below the table. Updated header and footer.	1/25/16

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.idt.com/go/support