

Features

- Clock doubler
- High-Performance Phase-Locked-Loop Clock Distribution for Networking, ATM, 100 MHz and 134 MHz Registered DIMM Synchronous DRAM modules for server, workstation, and PC applications
- Zero Input-to-Output delay
- Cycle-to-Cycle jitter $\leq \pm 150\text{ps}$ max.
- On-chip series damping resistor at clock output drivers for low noise and EMI reduction
- Operates at 3.3V V_{CC}
- Packaging (Pb-free & Green available):
 - 8-pin SOIC Package (W)

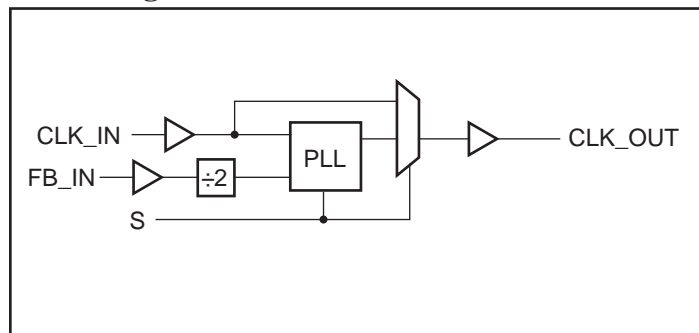
Description

The PI6C2402 features a low-skew, low-jitter, Phase-Locked Loop (PLL) clock driver. By connecting the feedback CLK_OUT output to the feedback FB_IN input, the propagation delay from the CLK_IN input to any clock output will be nearly zero. The PI6C2402 provides 2X CLK_IN on CLK_OUT output.

Applications

If the system designer needs more than 16 outputs with the features just described, using two or more zero-delay buffers such as the PI6C2509, and the PI6C2510, are likely to be impractical. The device-to-device skew introduced can significantly reduce the performance. Pericom recommends the use of a zero-delay buffer and an eighteen output non-zero delay buffer. As shown in Figure 1, this combination produces a zero-delay buffer with all the signal characteristics of the original zero-delay buffer, but with as many outputs as the non-zero-delay buffer part. For example, when combined with an eighteen output non-zero delay buffer, a system designer can create a seventeen-output zero-delay buffer.

Block Diagram



Pin Configuration

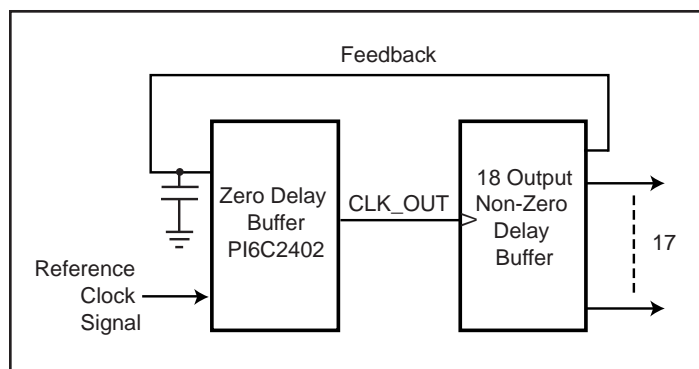
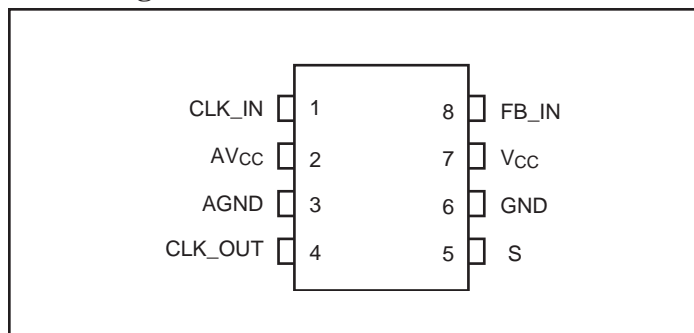


Figure 1. Zero-Delay Buffering Diagram

Control Input

S	Outputs Source	PLL Shutdown
HIGH	PLL	Disabled
LOW	CLK_IN	Enabled

Pin Functions

Name	Number	Type	Description
CLK_IN	1	I	Reference Clock input, CLK_IN allows spread spectrum clock input
AVCC	2	Power	Analog Power
AGND	3	Ground	Analog Ground
CLK_OUT	4	O	Clock Output. The output provides low-skew copies of CLK_IN and has an embedded series-damping resistor.
S	5	I	Control Input S. S is used to bypass the PLL for test purposes. When S is strapped to ground, PLL is bypassed and CLK_IN is buffered directly to the device outputs
GND	6	Ground	Ground
VCC	7	Power	Power Supply
FB_IN	8	I	Feedback input. FB_IN provides the feedback signal to the internal PLL.

Absolute Maximum Ratings⁽¹⁾ (Over operating free-air temperature range)

Symbol	Test Conditions	Min.	Max.	Units
V _I	Input voltage range	-0.5	V _{CC} + 0.5	V
V _O	Output voltage range	-0.5	V _{CC} + 0.5	
V _I _DC	DC input voltage	-0.5	5.0	
IO_DC	DC output current		100	mA
Power	Maximum power dissipation at TA = 55°C in still air		1.0	W
T _{STG}	Storage temperature	-65	150	°C

Note:

1. Stress beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

Recommended Operating Conditions

Symbol	Test Conditions	Temperature	Min.	Max.	Units
V _{CC}	Supply Voltage	Commercial	3.0	3.6	V
		Industrial	3.135	3.465	
V _{IH}	High Level input voltage		2.0		
V _{IL}	Low Level input voltage			0.8	
V _I	Input voltage		0	V _{CC}	
T _A	Operating free-air temperature	Commercial	0	70	°C
		Industrial	-40	85	

Electrical Characteristics

(Over recommended operating free-air temperature range)

Symbol	Test Conditions	Temperature	Condition	Min.	Typ.	Max.	Units
I _{CC}	V _I = GND; I _O = 0 ⁽¹⁾	Commercial	3.6V			10	μA
		Industrial	3.465V			10	
C _I	V _I = V _{CC} or GND		3.3V		4		pF
C _O	V _O = V _{CC} or GND		3.3V		6		
I _{OH}	V _{OUT} = 2.4V					-12	mA
	V _{OUT} = 2.0V					-18	
I _{OL}	V _{OUT} = 0.8V			18			
	V _{OUT} = 0.55V			12			

Note:

1. Continuous Output Current

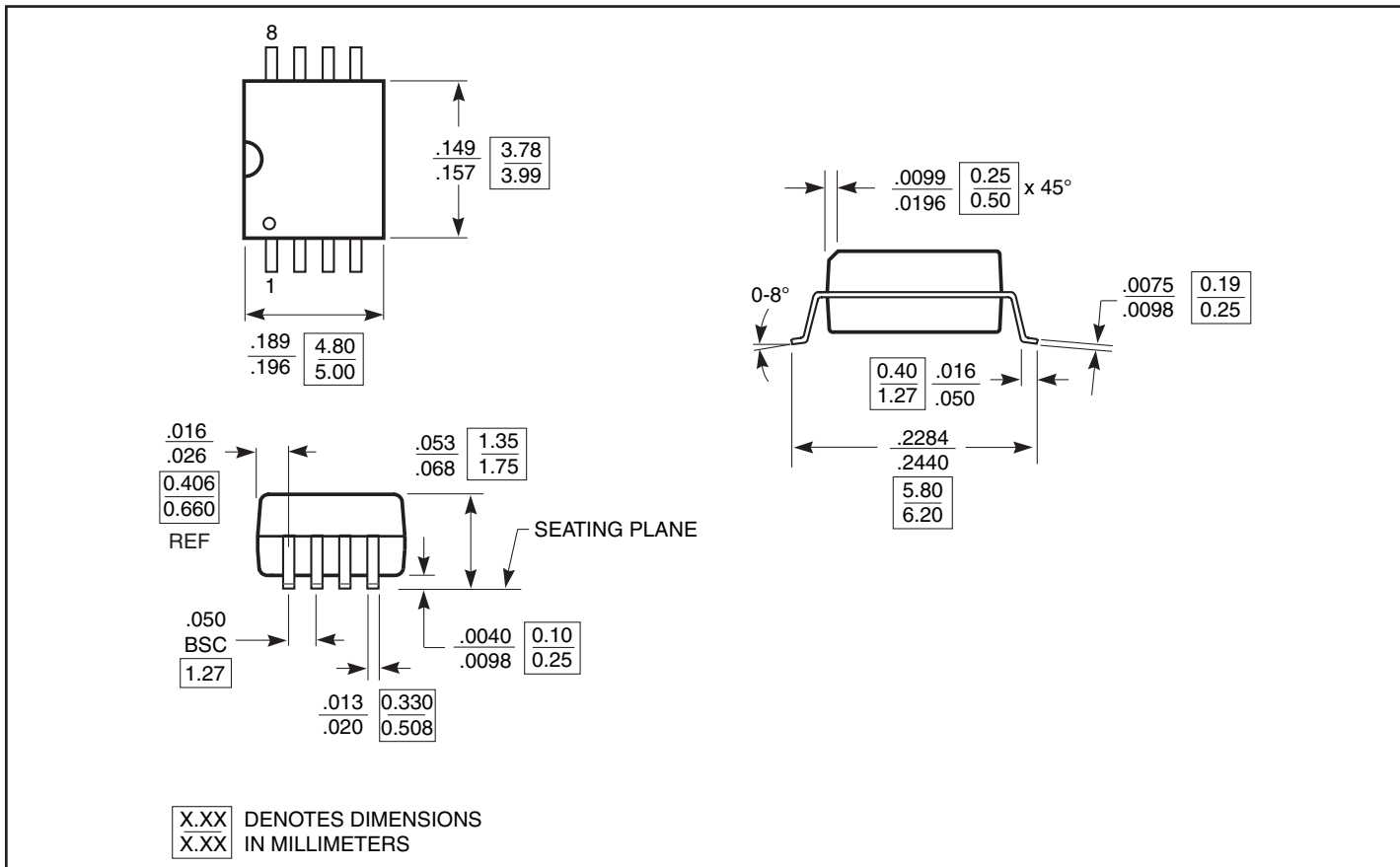
AC Specifications Timing Requirements

 (Over recommended ranges of supply voltage and operating free-air temperature, C_L = 25pF)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
F _{OUT}	Clock Frequency	Commercial	25		134	MHz
		Industrial	25		100	
D _{CYI}	Input clock duty cycle		40		60	%
	Stabilization time after power up				1	ms
t _p	Phase error without jitter ⁽¹⁾	CLK_IN↑ at 100 MHz and 66 MHz	-150		150	ps
t _j	Jitter, cycle-to-cycle	At 100 MHz	-150		150	
	Duty Cycle	At ≤ 100 MHz	45		55	%
		At > 100 MHz	35		65	
t _r	Rise-time 0.4V to 2.0V			1.0		ns
t _f	Fall-time 2.0V to 0.4V			1.1		

Note:

1. This switching parameter is guaranteed by design.

Packaging Mechanical: 8-pin Plastic SOIC (W)

Ordering Information(1,2,3)

Ordering Code	Package Code	Package Description
PI6C2402WE	W	Pb-free & Green, 8-pin, 150-mil SOIC

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel