

CMLDM8002A  
CMLDM8002AG\*  
CMLDM8002AJ

SURFACE MOUNT SILICON  
DUAL P-CHANNEL  
ENHANCEMENT-MODE  
MOSFETS



SOT-563 CASE

\* Device is **Halogen Free** by design



www.centrasemi.com

**DESCRIPTION:**

These CENTRAL SEMICONDUCTOR devices are dual chip P-Channel enhancement-mode MOSFETs, manufactured by the P-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM8002A utilizes the USA pinout configuration, while the CMLDM8002AJ, utilizing the Japanese pinout configuration, is available as a special order. These special dual transistor devices offer low  $r_{DS(on)}$  and low  $V_{DS(on)}$ .

**MARKING CODES:** CMLDM8002A: C08  
CMLDM8002AG\*: CG8  
CMLDM8002AJ: CJ8

**APPLICATIONS:**

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

**FEATURES:**

- Dual Chip Device
- Low  $r_{DS(on)}$
- Low  $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small SOT-563 package

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage	
Drain-Gate Voltage	
Gate-Source Voltage	
Continuous Drain Current	
Continuous Source Current (Body Diode)	
Maximum Pulsed Drain Current	
Maximum Pulsed Source Current	
Power Dissipation (Note 1)	
Power Dissipation (Note 2)	
Power Dissipation (Note 3)	
Operating and Storage Junction Temperature	
Thermal Resistance	

SYMBOL		UNITS
$V_{DS}$	50	V
$V_{DG}$	50	V
$V_{GS}$	20	V
$I_D$	280	mA
$I_S$	280	mA
$I_{DM}$	1.5	A
$I_{SM}$	1.5	A
$P_D$	350	mW
$P_D$	300	mW
$P_D$	150	mW
$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
$\theta_{JA}$	357	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS PER TRANSISTOR:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
$I_{GSS}, I_{GSSR}$	$V_{GS}=20\text{V}, V_{DS}=0$		100	nA
$I_{DSS}$	$V_{DS}=50\text{V}, V_{GS}=0$		1.0	$\mu\text{A}$
$I_{DSS}$	$V_{DS}=50\text{V}, V_{GS}=0, T_J=125^\circ\text{C}$		500	$\mu\text{A}$
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS}=10\text{V}$	500		mA
$BV_{DSS}$	$V_{GS}=0, I_D=10\mu\text{A}$	50		V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$		1.5	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		0.15	V
$V_{SD}$	$V_{GS}=0, I_S=115\text{mA}$		1.3	V

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm<sup>2</sup>  
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm<sup>2</sup>

R7 (8-June 2015)

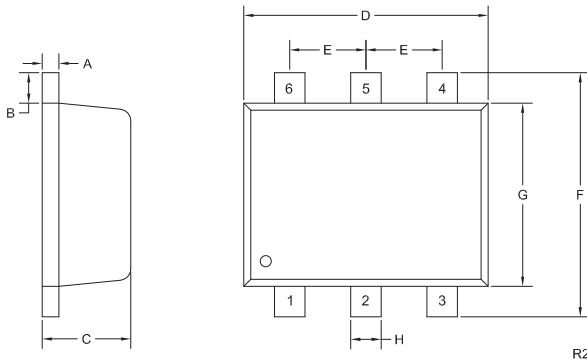
**CMLDM8002A**  
**CMLDM8002AG\***  
**CMLDM8002AJ**  
  
**SURFACE MOUNT SILICON**  
**DUAL P-CHANNEL**  
**ENHANCEMENT-MODE**  
**MOSFETS**



**ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$r_{DS(ON)}$	$V_{GS}=10V, I_D=500mA$			2.5	$\Omega$
$r_{DS(ON)}$	$V_{GS}=10V, I_D=500mA, T_J=125^\circ\text{C}$			4.0	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0V, I_D=50mA$			3.0	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0V, I_D=50mA, T_J=125^\circ\text{C}$			5.0	$\Omega$
g <sub>FS</sub>	$V_{DS}=10V, I_D=200mA$	200			mS
C <sub>rss</sub>	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$			7.0	pF
C <sub>iss</sub>	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$			70	pF
C <sub>oss</sub>	$V_{DS}=25V, V_{GS}=0, f=1.0MHz$			15	pF
Q <sub>g(tot)</sub>	$V_{DS}=25V, V_{GS}=4.5V, I_D=100mA$		0.72		nC
Q <sub>gs</sub>	$V_{DS}=25V, V_{GS}=4.5V, I_D=100mA$		0.25		nC
Q <sub>gd</sub>	$V_{DS}=25V, V_{GS}=4.5V, I_D=100mA$		0.16		nC
t <sub>on</sub> , t <sub>off</sub>	$V_{DD}=30V, V_{GS}=10V, I_D=200mA$ $R_G=25\Omega, R_L=150\Omega$			20	ns

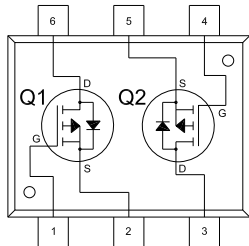
**SOT-563 CASE - MECHANICAL OUTLINE**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0027	0.007	0.07	0.18
B		0.008		0.20
C	0.017	0.024	0.45	0.60
D	0.059	0.067	1.50	1.70
E		0.020		0.50
F	0.059	0.067	1.50	1.70
G	0.043	0.051	1.10	1.30
H	0.006	0.012	0.15	0.30

SOT-563 (REV: R2)

**CMLDM8002A (USA Pinout)**  
**CMLDM8002AG\***



**LEAD CODE:**

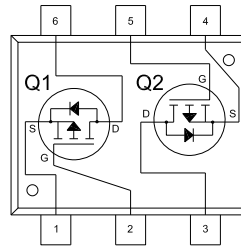
- 1) Gate Q1
- 2) Source Q1
- 3) Drain Q2
- 4) Gate Q2
- 5) Source Q2
- 6) Drain Q1

**MARKING CODES:**

**CMLDM8002A: C08**  
**CMLDM8002AG\*: CG8**

\* Device is *Halogen Free* by design

**CMLDM8002AJ (Japanese Pinout)**



**LEAD CODE:**

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

**MARKING CODE: CJ8**

R7 (8-June 2015)

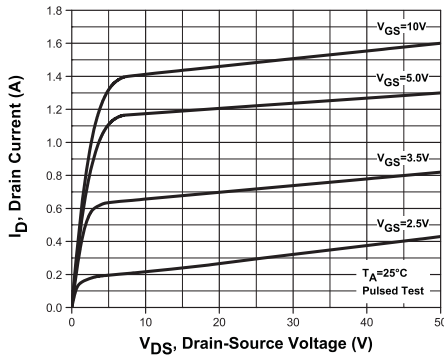
CMLDM8002A  
 CMLDM8002AG\*  
 CMLDM8002AJ

SURFACE MOUNT SILICON  
 DUAL P-CHANNEL  
 ENHANCEMENT-MODE  
 MOSFETS

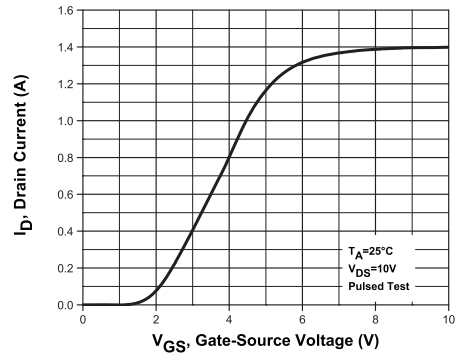


TYPICAL ELECTRICAL CHARACTERISTICS

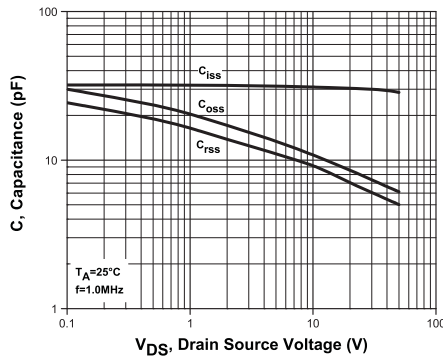
Output Characteristics



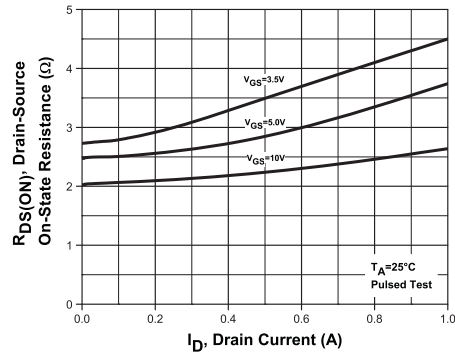
Transfer Characteristics



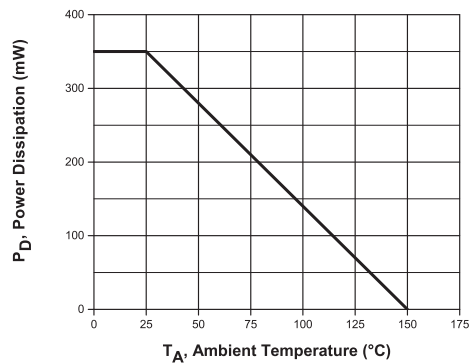
Capacitance



Drain Source On Resistance



Power Derating



R7 (8-June 2015)

## OUTSTANDING SUPPORT AND SUPERIOR SERVICES



---

### PRODUCT SUPPORT

Central's operations team provides the highest level of support to insure product is delivered on-time.

- Supply management (Customer portals)
- Inventory bonding
- Consolidated shipping options
- Custom bar coding for shipments
- Custom product packing

---

### DESIGNER SUPPORT/SERVICES

Central's applications engineering team is ready to discuss your design challenges. Just ask.

- Free quick ship samples (2<sup>nd</sup> day air)
- Online technical data and parametric search
- SPICE models
- Custom electrical curves
- Environmental regulation compliance
- Customer specific screening
- Up-screening capabilities
- Special wafer diffusions
- PbSn plating options
- Package details
- Application notes
- Application and design sample kits
- Custom product and package development

---

### CONTACT US

#### Corporate Headquarters & Customer Support Team

Central Semiconductor Corp.  
145 Adams Avenue  
Hauppauge, NY 11788 USA  
Main Tel: (631) 435-1110  
Main Fax: (631) 435-1824  
Support Team Fax: (631) 435-3388  
[www.centalsemi.com](http://www.centalsemi.com)

**Worldwide Field Representatives:**  
[www.centalsemi.com/wwreps](http://www.centalsemi.com/wwreps)

**Worldwide Distributors:**  
[www.centalsemi.com/wwdistributors](http://www.centalsemi.com/wwdistributors)

---

For the latest version of Central Semiconductor's **LIMITATIONS AND DAMAGES DISCLAIMER**, which is part of Central's Standard Terms and Conditions of sale, visit: [www.centalsemi.com/terms](http://www.centalsemi.com/terms)