Technical Summary

MPC875TS
Rev. 2.0, 12/2003

MPC875/MPC870
PowerQUICC™ Family
Technical Summary

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This document provides an overview of the MPC875 PowerQUICC™ family, describing major functions and features.

The MPC875 PowerQUICC family contains a PowerPC™ processor core. It is a 0.18-micron version of the MPC860 PowerQUICC family and can operate up to 133 MHz (2:1 mode) on the MPC8xx core and up to 80 MHz (1:1 mode) on the external bus. It has a 1.8-V core and a 3.3-V I/O operation with a 5-V TTL compatibility. The MPC875 integrated communications controller family is a versatile single-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications. It particularly excels in both communications and networking systems.

The MPC875 family is a PowerPC architecture-based quad integrated communications controller (PowerQUICC). The CPU on the MPC875 has a MPC8xx core, a 32-bit microprocessor that implements the PowerPC architecture, incorporating memory management units (MMUs) and instruction and data caches. The MPC875 is a superset of this lower cost family of devices and is the main focus of this document.

Table 1 shows the functionality supported by the members of the MPC875 family:

Table 1. MPC875 Family

Part	Cache		Ethernet		SCC	SMC	USB	Security Engine
	I Cache	D Cache	10BaseT	10/100				
MPC875	8 Kbyte	8 Kbyte	Up to 1	2	1	1	1	Yes
MPC870	8 Kbyte	8 Kbyte	—	2	—	1	1	No

1 Features

The MPC875 family is comprised of three modules that each use the 32-bit internal bus: a MPC8xx core, a system integration unit (SIU), and a communication processor module (CPM).

The following list summarizes the key MPC875 family features:

- Embedded MPC8xx core up to 133 MHz
- Maximum frequency operation of the external bus is 80 MHz (in 1:1 mode)
  - The 133-MHz core frequency supports 2:1 mode only.
  - The 66-/80-MHz core frequencies support both 1:1 and 2:1 modes.
- Single-issue, 32-bit core (compatible with the PowerPC architecture definition) with thirty-two 32-bit general-purpose registers (GPRs)
  - The core performs branch prediction with conditional prefetch, without conditional execution.
  - 8-Kbyte data cache and 8-Kbyte instruction cache (see Table 1)
    - 8-Kbyte instruction cache is two-way, set-associative with 256 sets in 2 blocks
    - 8-Kbyte data cache is two-way, set-associative with 256 sets
    - Cache coherency for both instruction and data caches is maintained on 128-bit (4-word) cache blocks.
    - Caches are physically addressed, implement a least recently used (LRU) replacement algorithm, and are lockable on a cache block basis.
  - MMUs with 32-entry TLB, fully associative instruction and data TLBs
  - MMUs support multiple page sizes of 4, 16, and 512 Kbytes, and 8 Mbytes; 16 virtual address spaces and 16 protection groups.
  - Advanced on-chip emulation debug mode
- Up to 32-bit data bus (dynamic bus sizing for 8, 16, and 32 bits)
- Thirty-two address lines
- Memory controller (eight banks)
  - Contains complete dynamic RAM (DRAM) controller
  - Each bank can be a chip select or $\overline{\text{RAS}}$ to support a DRAM bank
  - Up to 30 wait states programmable per memory bank
  - Glueless interface to DRAM, SIMMS, SRAM, EPROMs, Flash EPROMs, and other memory devices
  - DRAM controller programmable to support most size and speed memory interfaces
  - Four $\overline{\text{CAS}}$ lines, four $\overline{\text{WE}}$ lines, and one $\overline{\text{OE}}$ line
  - Boot chip-select available at reset (options for 8-, 16-, or 32-bit memory)
  - Variable block sizes (32 Kbyte–256 Mbyte)
  - Selectable write protection
  - On-chip bus arbitration logic
- General-purpose timers
  - Four 16-bit timers or two 32-bit timers
  - Gate mode can enable/disable counting
  - Interrupt can be masked on reference match and event capture
- Two fast Ethernet controllers (FEC)—Two 10/100 Mbps Ethernet/IEEE 802.3 CDMA/CS that interface through MII and/or RMII interfaces

- System integration unit (SIU)
  - Bus monitor
  - Software watchdog
  - Periodic interrupt timer (PIT)
  - Clock synthesizer
  - Decrementer and time base
  - Reset controller
  - IEEE 1149.1 test access port (JTAG)
- Security engine is optimized to handle all the algorithms associated with IPsec, SSL/TLS, SRTP, 802.11i, and iSCSI processing. Available on the MPC875, the security engine contains one crypto-channel, a controller, and a set of crypto hardware accelerators (CHAs). The CHAs are:
  - Data encryption standard execution unit (DEU)
    - DES, 3DES
    - Two key (K1, K2, K1) or three key (K1, K2, K3)
    - ECB and CBC modes for both DES and 3DES
  - Advanced encryption standard unit (AESU)
    - Implements the Rijndael symmetric key cipher
    - ECB, CBC, and counter modes
    - 128-, 192-, 256-bit key lengths
  - Message digest execution unit (MDEU)
    - SHA with 160- or 256-bit message digest
    - MD5 with 128-bit message digest
    - HMAC with either algorithm
  - Master/slave logic, with DMA
    - 32-bit address/32-bit data
    - Operation at 8xx bus frequency
  - Crypto-channel supporting multi-command descriptors
    - Integrated controller managing crypto-execution units
    - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Interrupts
  - Six external interrupt request (IRQ) lines
  - Twelve port pins with interrupt capability
  - 23 internal interrupt sources
  - Programmable priority between SCCs
  - Programmable highest priority request
- Communications processor module (CPM)
  - RISC controller
  - Communication-specific commands (for example, GRACEFUL STOP TRANSMIT, ENTER HUNT MODE, and RESTART TRANSMIT)
  - Supports continuous mode transmission and reception on all serial channels
  - 8-Kbytes of dual-port RAM
  - Several serial DMA (SDMA) channels to support the CPM
  - Three parallel I/O registers with open-drain capability

- On-chip 16 x 16 multiply accumulate controller (MAC)
  - — One operation per clock (two clock latency, one clock blockage)
  - — MAC operates concurrently with other instructions
  - — FIR loop—Four clocks per four multiplies
- Four baud rate generators
  - — Independent (can be connected to any SCC or SMC)
  - — Allow changes during operation
  - — Autobaud support option
- The MPC875 has one SCC (serial communication controller)
  - — Ethernet/IEEE 802.3 optional on the SCC, supporting full 10-Mbps operation
  - — HDLC/SDLC
  - — HDLC bus (implements an HDLC-based local area network (LAN))
  - — Asynchronous HDLC to support PPP (point-to-point protocol)
  - — AppleTalk
  - — Universal asynchronous receiver transmitter (UART)
  - — Synchronous UART
  - — Serial infrared (IrDA)
  - — Binary synchronous communication (BISYNC)
  - — Totally transparent (bit streams)
  - — Totally transparent (frame based with optional cyclic redundancy check (CRC))
- SMC (serial management channel)
  - — UART (low-speed operation)
  - — Transparent
- Universal serial bus (USB)—Supports operation as a USB function endpoint, a USB host controller, or both for testing purposes (loopback diagnostics)
  - — USB 2.0 full-/low-speed compatible
  - — The USB function mode features are as follows:
    - – Four independent endpoints support control, bulk, interrupt, and isochronous data transfers
    - – CRC16 generation and checking
    - – CRC5 checking
    - – NRZI encoding/decoding with bit stuffing
    - – 12- or 1.5-Mbps data rate
    - – Flexible data buffers with multiple buffers per frame
    - – Automatic retransmission upon transmit error
  - — The USB host controller features are as follows:
    - – Supports control, bulk, interrupt, and isochronous data transfers
    - – CRC16 generation and checking
    - – NRZI encoding/decoding with bit stuffing
    - – Supports both 12- and 1.5-Mbps data rates (automatic generation of preamble token and data rate configuration). Note that low-speed operation requires an external hub.
    - – Flexible data buffers with multiple buffers per frame
    - – Supports local loopback mode for diagnostics (12 Mbps only)

- SPI (serial peripheral interface)
  - — Supports master and slave modes
  - — Supports multiple-master operation on the same bus
- I^2C (inter-integrated circuit) port
  - — Supports master and slave modes
  - — Supports a multiple-master environment
- Time-slot assigner (TSA) that supports one TDM bus (TDMb)
  - — Allows SCC and SMC to run in multiplexed and/or non-multiplexed operation
  - — Supports T1, CEPT, PCM highway, ISDN basic rate, ISDN primary rate, user defined
  - — 1- or 8-bit resolution
  - — Allows independent transmit and receive routing, frame synchronization, and clocking
  - — Allows dynamic changes
  - — Can be internally connected to two serial channels (one SCC and one SMC)
- PCMCIA interface
  - — Master (socket) interface, PCI 2.1-compliant
  - — Supports one independent PCMCIA socket on the MPC875/MPC870
  - — Eight memory or I/O windows supported
- Debug interface
  - — Eight comparators: four operate on instruction address, two operate on data address, and two operate on data.
  - — Supports conditions: = ≠ < >
  - — Each watchpoint can generate a breakpoint internally
- Normal high and normal low power modes to conserve power
- 1.8-V core and 3.3-V I/O operation with 5-V TTL compatibility
- The MPC875/MPC870 comes in a 256-pin ball grid array (PBGA) package.

Features

The MPC875 block diagram is shown in Figure 1.

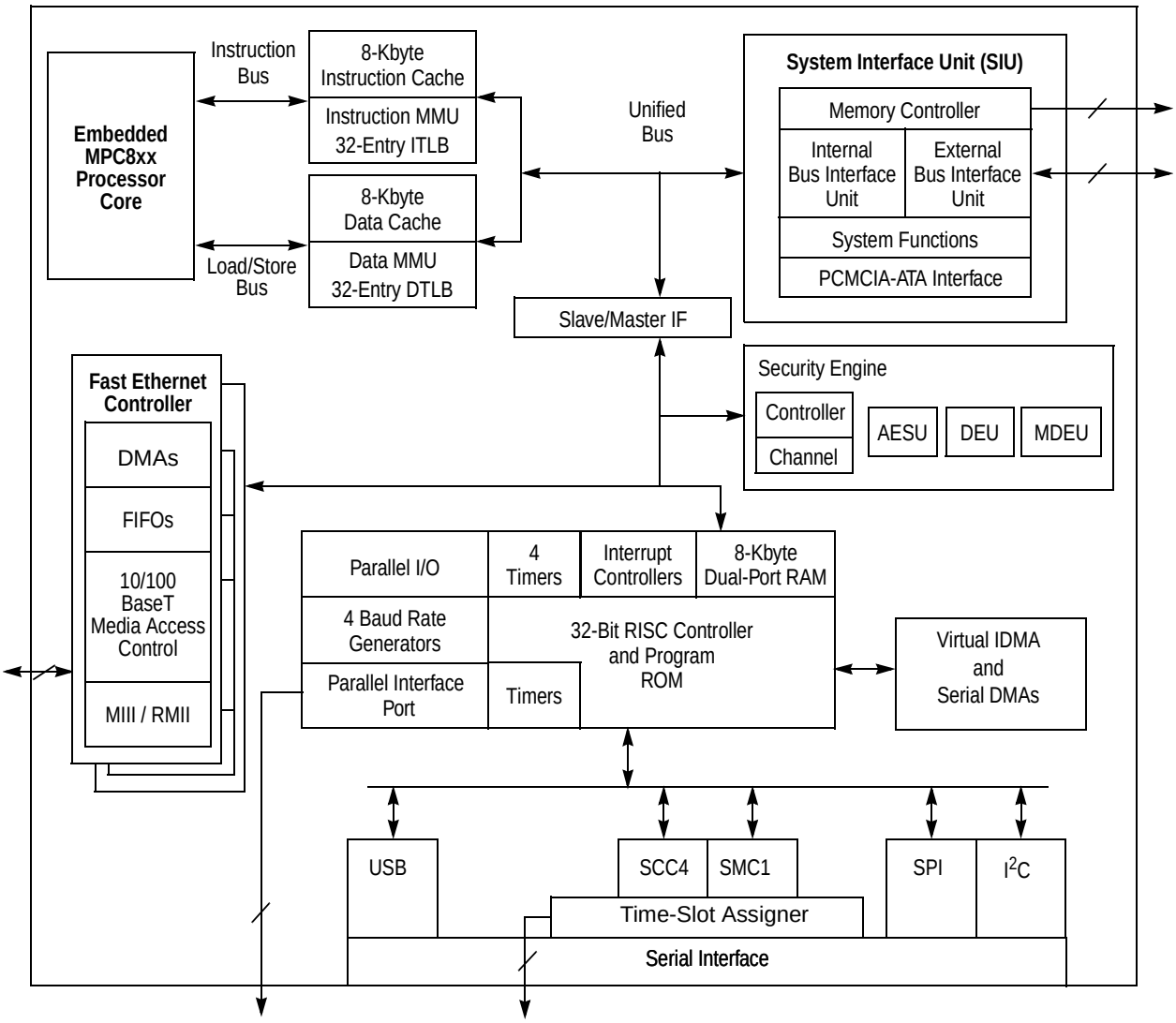

Figure 1. MPC875 Block Diagram

The MPC870 block diagram is shown in Figure 2.

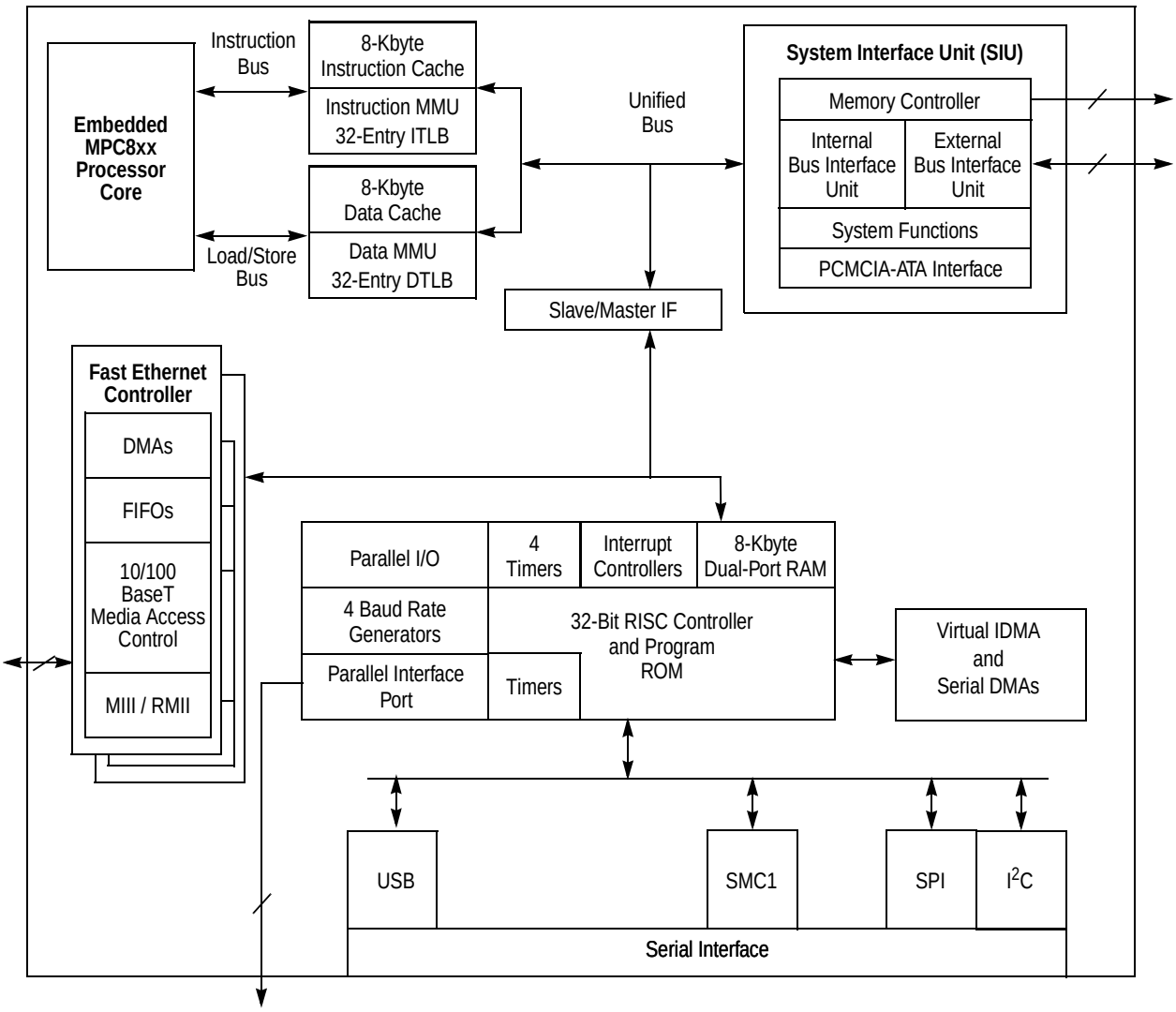

Figure 2. MPC870 Block Diagram

2 Embedded MPC8xx Core

The MPC875 family integrates an embedded MPC8xx core with high-performance, low-power peripherals to extend the Motorola data communications family of embedded processors further into high-end communications and networking products.

The core is compliant with the UISA (user instruction set architecture) portion of the PowerPC architecture. It has an integer unit (IU) and a load/store unit (LSU) that execute all integer and load/store operations in the hardware. The core supports integer operations on a 32-bit internal data path and 32-bit arithmetic hardware. The core interface to the internal and external buses is 32 bits.

The IU uses thirty-two 32-bit GPRs for source and target operands. Typically, it can execute one integer instruction per clock cycle. Each element in the integer block is clocked only when valid data is in the data queue and is ready for operation. This holds power consumption of the device to the absolute minimum.

The core is integrated with MMUs as well as instruction and data caches. Each MMU provides a 32-entry, fully-associative instruction and data TLB, with multiple page sizes of 4, 16, 512, and 256 Kbytes and 8 Mbytes. It supports 16 virtual address spaces with 8 protection groups. Three special scratch registers support software table search and update operations.

The instruction cache is two-way, set-associative with physical addressing. It allows single-cycle access on hits with no added latency for misses. It has four words per block, supporting a four-beat burst line fill using an LRU (least recently used) replacement algorithm. The cache can be locked on a per cache block basis for application-critical routines.

The data cache is two-way, set-associative with physical addressing. It allows single-cycle accesses on hits with one added clock latency for misses. It has four words per cache block, supporting burst line fill using LRU replacement. The cache can be locked on a per block basis for application critical routines. The data cache can be programmed through the MMU to support copy back or write through. Cache-inhibit mode can be programmed per MMU page.

The debug interface provides debug capabilities without degrading operation speed. This interface supports six watchpoint pins that are used to detect software events. Four of its eight internal comparators operate on the effective address on the address bus, two operate on the effective address on the data address bus, and two operate on the data bus. The core can make =, ≠, <, and > comparisons to generate watchpoints. Each watchpoint can then generate a break point that can be configured to trigger in a programmable number of events.

3 System Interface Unit (SIU)

The SIU on the MPC875 family integrates general-purpose features useful in almost any 32-bit processor system. Dynamic bus sizing allows 8-, 16-, and 32-bit peripherals and memory to exist in the 32-bit system bus mode.

The SIU also provides power management functions, reset control, a decrementer, and a time base.

The memory controller supports up to eight memory banks with glueless interfaces to DRAM, SRAM, SSRAM, EPROM, Flash EPROM, SDRAM, EDO, and other peripherals with 2-clock cycle access to external SRAM and bursting support. It provides variable block sizes from 32 Kbytes to 256 Mbytes. The memory controller provides 0–30 wait states for each memory bank and can use address type matching to qualify each memory bank access. It provides four byte-enable signals, an output-enable signal, and a boot chip select available at reset.

The DRAM interface supports port sizes of 8, 16, and 32 bits. Memory banks can be defined in depths of 256 or 512 Kbytes or 1, 2, 4, 8, 16, 32, or 64 Mbytes for all port sizes. The memory depth can be 64 and 128 Kbytes for 8-bit memory or 128 and 256 Mbytes for 32-bit memory. The DRAM controller supports page-mode access for successive transfers within bursts. The MPC875 supports a glueless interface to one bank of DRAM while external buffers are required for additional memory banks. The refresh unit provides $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$, a programmable refresh timer, refresh active during external reset, disable refresh mode, and stacking up to seven refresh cycles. The DRAM interface uses a programmable state machine to support almost any memory interface.

4 PCMCIA Controller

The PCMCIA interface is a master (socket) controller and is PCI 2.1-compliant. The interface supports one independent PCMCIA socket requiring only external transceivers/buffers. The interface provides eight memory or I/O windows, where each window can be allocated to a particular socket.

5 Power Management

The MPC875 family supports two power management features including normal high and normal low power modes. Full-on mode leaves the MPC875 processor fully powered with all internal units operating at full processor speed. A gear mode is determined by a clock divider, allowing the operating system to reduce the processor's operational frequency and operate in normal low mode.

6 Security Engine

A block diagram of the security engine's internal architecture is shown in Figure 3. The MPC8xx bus interface (8xx/IF) module is designed to transfer 32-bit words between the MPC8xx bus and any register inside the security engine core.

An operation begins with a write of a pointer to the crypto-channel fetch register, which points to a data packet descriptor. The channel requests the descriptor and decodes the operation to be performed. The channel then requests the controller to assign crypto-execution units and fetch the keys, IVs, and data needed to perform the given operation. The controller satisfies the requests by assigning execution units to the channel and by making requests to the master interface. As data is processed, it is written to the individual execution unit's output buffer and then back to system memory through the 8xx/IF module.

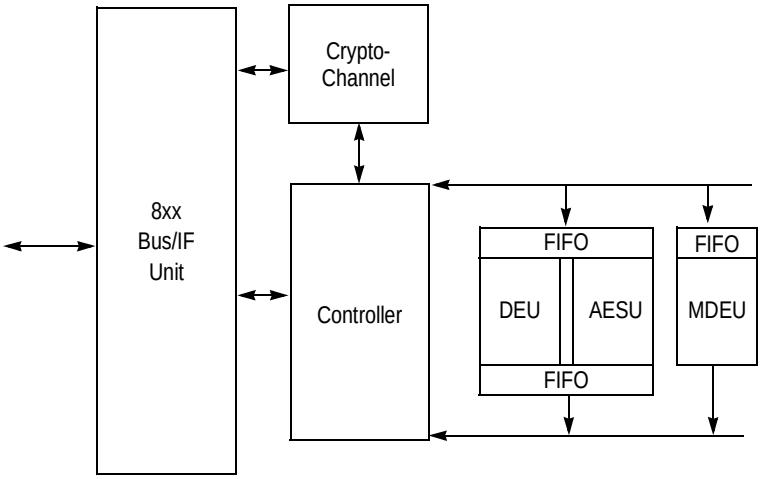

Figure 3. Security Engine Functional Blocks

7 Fast Ethernet Controller (FEC)

The FECs comply with the IEEE 802.3 specification for 10- and 100-Mbps connectivity. Full-duplex 100-Mbps operation is supported at system clock rates of 40 MHz and higher. A 25-MHz system clock supports 10-Mbps operation or half-duplex 100-Mbps operation.

The implementation of bursting DMA reduces bus usage. Independent DMA channels for accessing BDs and transmit and receive data minimize latency and FIFO depth requirements.

Transmit and receive FIFOs further reduce bus usage by localizing all collisions to the FEC. Transmit FIFOs maintain a full collision window of transmit frame data, eliminating the need for repeated DMA over the system bus when collisions occur. On the receive side, a full collision window of data is received before any receive data is transferred into system memory, allowing the FIFO to be flushed in the event of a runt or collided frame, with no DMA activity. However, external memory for buffers and BDs is required; on-chip FIFOs are designed only to compensate for collisions and system bus latency.

Independent TxBD and RxBD rings in external memory allow nearly unlimited flexibility in memory management of transmit and receive data frames. External memory is inexpensive, and because BD rings in external memory have no inherent size limitations, memory management can be easily optimized to system needs.

8 Universal Serial Bus (USB)

The universal serial bus (USB) is an industry-standard extension to the PC architecture. The USB controller on the MPC875 family supports data exchange between a wide range of simultaneously accessible peripherals. Attached peripherals share USB bandwidth through a host-scheduled, token-based protocol.

The USB physical interconnect is a tiered-star topology, and the center of each star is a hub. Each wire segment is a point-to-point connection between the host and a hub or function, or a hub connected to another hub or function. The USB transfers signal and power over a four-wire cable, and the signaling occurs over two wires and point-to-point segments. The USB full speed signaling bit rate is 12 Mbps. Also, a limited capability low speed signaling mode is defined at 1.5 Mbps. Refer to revisions 1.1 and 2.0 of the *USB Specification* for further details. They can be downloaded from http://www.usb.org.

The MPC875 USB controller consists of a transmitter module, receiver module, and two protocol state machines. The protocol state machines control the receiver and transmitter modules. One state machine implements the function state diagram, and the other implements the host state diagram. The USB controller can implement a USB function endpoint, a USB host, or both for testing purposes (loopback diagnostics).

9 Communications Processor Module (CPM)

The MPC875 family is the next generation MPC8xx family of devices. Like its predecessor, it implements a dual-processor architecture, which provides both a high-performance, general-purpose processor for application programming use and a special-purpose communication processor (CPM) uniquely designed for communications applications.

The CPM contains features that, like its predecessor, allow the MPC875 family to excel in communications and networking products. These features are grouped as follows:

- Communications processor (CP)
- Independent DMA (SDMA) controllers
- Four general-purpose timers

The CP provides the communication features of the MPC875 family. Included are a RISC processor, one serial communication controller (SCC), one serial management controller (SMC), a serial peripheral interface (SPI), an I^2C interface, 8 Kbytes of dual-port RAM, an interrupt controller, a time-slot assigner (TSA), five parallel ports, four independent baud rate generators, and serial DMA channels to support the SCC, SMC, and SPI.

The SDMAs provide two channels of general-purpose DMA capability for each communications channel. They offer high-speed transfers, 32-bit data movement, buffer chaining, and independent request and acknowledge logic.

The four general-purpose timers on the CPM are identical to the timers found on all of the MPC8xx devices and support the internal cascading of two timers to form a 32-bit timer.

10 Revision History

Table 2 provides a revision history for this document.

Table 2. Revision History

Revision Number	Date	Change
0	01/2003	Initial document.
0.1	02/2003	Added 5-V capability.
0.2	03/2003	Modified the first three bullets and removed the time-slot assigner from the Features list and removed the questions with question marks.
0.3	03/2003	Removed question on interrupts, added Preliminary.
0.4	05/2003	Put in the new Features list, put I^2C back in.
0.5	8/2003	Added reference to USB 2.0 to the Features list and removed 1.1 from USB Figures 1 and 2. Added USB 2.0 to Section 8, “Universal Serial Bus (USB)”.
0.6	8/2003	Changed USB description to full-/low-speed compatible.
1.0	9/2003	Added DSP information in the Features list. Released to the external web.
1.1	10/2003	Added the TDMb to the MPC875 Features, the MPC875 Block Diagram.
2.0	12/2003	Changed the Maximum operating frequency to 133 MHz.

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