NCP1126, NCP1129

Product Preview

High Voltage Switcher for Offline Power Supplies

The NCP1126/NCP1129 switcher offers everything needed to build reliable and compact AC−DC switching power supplies with minimal surrounding elements. Incorporating a rugged 650 V MOSFET, converters built with the NCP112X can be safely designed for international conditions without jeopardizing the overall reliability. The NCP112X implements peak current mode control with adjustable ramp compensation that ensures stability in Continuous Conduction Mode (CCM) operation. With an external resistor, the maximum peak current is adjustable, allowing the designer the ability to inject ramp compensation to stabilize CCM power supplies.

A short circuit fault condition is independently detected from the auxiliary winding voltage resulting in improved short circuit protection with true overload detection. The Source pin provides access to the MOSFET source, allowing for overpower compensation.

With a supply range up to 26 V, the switcher also provides a jittered 65 kHz or 100 kHz switching frequency operated in peak current mode control. When the power on the secondary side starts to decrease, the switcher automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current.

Features

- 650 V Avalanche Rated MOSFET (2 Ω NCP1129 / 6 Ω NCP1126)
- Fixed−Frequency 65 or 100 kHz Current−Mode Control Operation
- Frequency Foldback Down to 26 kHz and Skip−Cycle in Light Load Conditions
- Adjustable Current Limit
- Internal Ramp Compensation
- Internal Fixed 4 ms Soft−Start
- 200 ms Timer−Based Auto−Recovery Short−Circuit Protection
- Frequency Jittering in Normal and Frequency Foldback Modes
- Option for Auto−Recovery or Latched Short−Circuit Protection
- Up to 26 V V_{CC} Operation
- Less than 100 mW Standby Power at High Line
- EPS 2.0 Compliant
- 7−Pin Package Provides Creepage Distance
- These are Pb−Free Devices

Typical Applications

- Power Supplies for DVDs, CD Players, Set Top Boxes, TVs
- Auxiliary Power Supplies (USB, Appliances, TVs)

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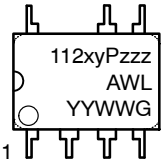
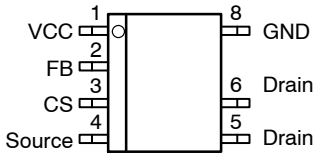
PDIP−7
P SUFFIX
CASE 626B

MARKING DIAGRAM



x	= Specific Device Code 6 = NCP1126 9 = NCP1129
y	= A or B A = Latch B = Auto−recovery
zzz	= Frequency 65 = 65 kHz 100 = 100 kHz
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

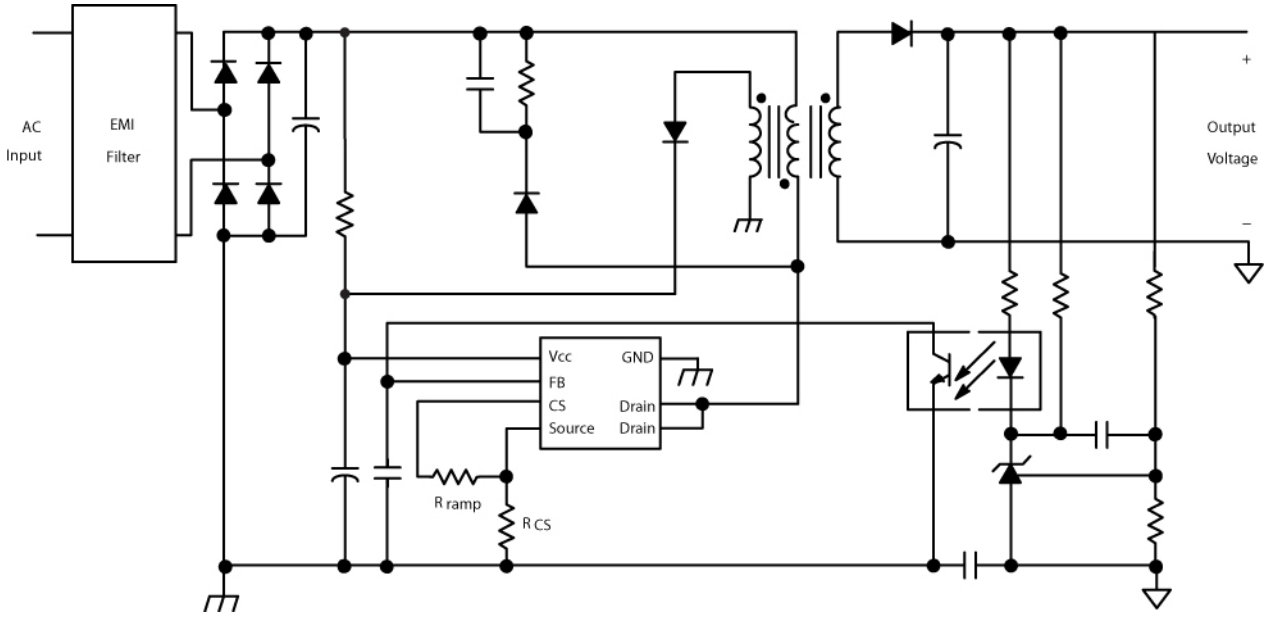


Figure 1. Typical Application Circuit

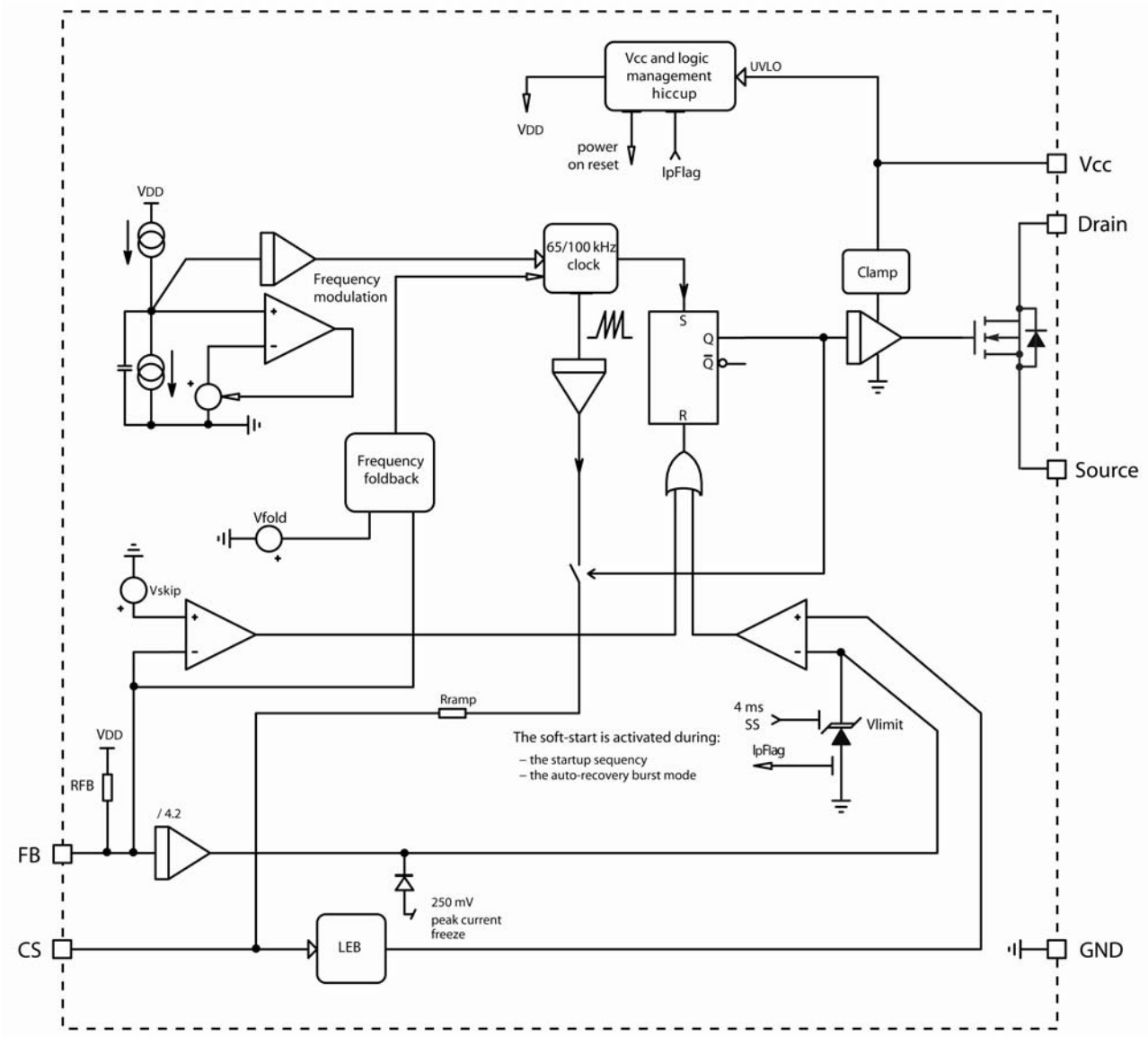


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Description
1	VCC	Supply input.
2	FB	Feedback input for the Flyback switcher. Allowed direct connection to an optocoupler.
3	CS	Input to the cycle−by−cycle current limit comparator for the Flyback section.
4	Source	This pin routes the MOSFET source to a grounded sense resistor and develops a voltage proportional to the drain current. These pins are internally connected.
5	Drain	These pins connect to the transformer terminal and withstand up to 650 V.
6	Drain	
7	–	Removed for creepage distance.
8	GND	Ground reference.

Table 2. OPTIONS AND ORDERING INFORMATION

Device	Frequency	Short−Circuit Protection	Package	Shipping†
NCP1126AP65G	65 kHz	Latch	PDIP−7 (Pb−Free)	TBD
NCP1126BP65G	65 kHz	Auto−Recovery	PDIP−7 (Pb−Free)	TBD
NCP1126AP100G	100 kHz	Latch	PDIP−7 (Pb−Free)	TBD
NCP1126BP100G	100 kHz	Auto−Recovery	PDIP−7 (Pb−Free)	TBD
NCP1129AP65G	65 kHz	Latch	PDIP−7 (Pb−Free)	TBD
NCP1129BP65G	65 kHz	Auto−Recovery	PDIP−7 (Pb−Free)	TBD
NCP1129AP100G	100 kHz	Latch	PDIP−7 (Pb−Free)	TBD
NCP1129BP100G	100 kHz	Auto−Recovery	PDIP−7 (Pb−Free)	TBD

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 3. MAXIMUM RATINGS TABLE (Notes 1, 2, 3 and 4)

Rating	Symbol	Value	Unit
Drain Input Voltage (Referenced to Source Terminal)	V_{Drain}	−0.3 to 650	V
Drain Maximum Continuous Current (T_J = 25°C) NCP1129 NCP1126	$I_{Drain(MAX)}$	 5.5 1.8	A
Single Pulse Avalanche Energy	E_{AS}	20	mJ
Source Input Voltage	V_{Source}	−0.3 to 7	V
Source Input Current	I_{Source}	$I_{Drain(MAX)}$	mA
Supply Input Voltage	$V_{CC(MAX)}$	−0.3 to 35	V
Supply Input Current	$I_{CC(MAX)}$	TBD	mA
Current Sense Input Voltage	V_{CS}	−0.3 to 10	V
Current Sense Input Current	I_{CS}	TBD	mA
Feedback Input Voltage	V_{FB}	−0.3 to 10	V
Feedback Input Current	I_{FB}	TBD	mA
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Power Dissipation (T_A = 25°C, 2 Oz Cu, 600 mm^2 Printed Circuit Copper Clad)	P_D	1.5	W
Thermal Resistance, Junction to Ambient 2 Oz Cu Printed Circuit Copper Clad) Low Conductivity High Conductivity	$R_{\theta JA}$	 128 78	°C/W
ESD Capability (Note 4) Human Body Model per JEDEC Standard JESD22−A114E. Machine Model per JEDEC Standard JESD22−A114E. Charge Device Model per JEDEC Standard JESD22−C101E.		 2000 200 2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device contains Latch−Up protection and exceeds ±100 mA per JEDEC Standard JESD78.
2. Low Conductivity Board. As mounted on 40 x 40 x 1.5 mm FR4 substrate with a single layer of 50 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection of zero air flow.
3. High Conductivity Board. As mounted on 40 x 40 x 1.5 mm FR4 substrate with a single layer of 600 mm^2 of 2 oz copper trances and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection of zero air flow.
4. The Drain pins (5 and 6), are rated to the maximum voltage of the device, or 650 V.

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage Startup Threshold Minimum Operating Voltage Operating Hysteresis	 V_{CC} increasing V_{CC} decreasing $V_{CC(on)} - V_{CC(off)}$	 $V_{CC(on)}$ $V_{CC(off)}$ $V_{CC(HYS)}$	 16 8.2 6.0	 18 8.8 –	 20 9.4 –	V
V_{CC} Overvoltage Protection Threshold		$V_{CC(OVP)}$	26.0	27.5	29.0	V
V_{CC} Overvoltage Protection Filter Delay		$t_{OVP(delay)}$	–	20	–	μs
V_{CC} Clamp Voltage in Latch Mode	I_{CC} = 500 μA	V_{ZENER}	–	7	–	V
Supply Current Startup Current Skip Current Operating Current at 65 kHz Operating Current at 100 kHz	 $V_{CC} = V_{CC(on)} - 0.5$ V V_{FB} = TBD V I_{FB} = 50 μA, f_{SW} = 65 kHz I_{FB} = 50 μA, f_{SW} = 100 kHz	 I_{CC1} I_{CC2} I_{CC3} I_{CC4}	 – – – –	 – 550 2100 2600	 15 TBD 3000 TBD	μA
Current Consumption in Latch Mode	T_J = 0°C to 125°C T_J = −40°C to 125°C	$I_{CC(latch1)}$ $I_{CC(latch2)}$	32 40	– –	– –	μA
SCR Current Limiting Resistor		R_{lim}	–	4	–	kΩ
POWER SWITCH CIRCUIT						
Off−State Leakage Current	T_J = 25°C, V_{Drain} = 650 V 25°C < T_J < 125°C, V_{Drain} = 650 V	$I_{Drain(off)}$	– –	– –	20 TBD	μA
Breakdown Voltage	T_J = 25 °C, I_{Drain} = 1 mA, V_{FB} = 0 V	$V_{BR(DSS)}$	650	–	–	V
ON State Resistance NCP1129 NCP1126	Voltage Supply = 5 V, R_{Drain} = 33 Ω V_{CC} = 10 V, T_J = 25°C V_{CC} = 10 V, T_J = 125°C V_{CC} = 10 V, T_J = 25°C V_{CC} = 10 V, T_J = 125°C	$R_{DS(on)}$	 – – – –	 2.1 – 6.0 –	 2.5 5.0 7.0 11	Ω
Output Capacitance NCP1129 NCP1126	 V_{DS} = 25 V, V_{CC} = 0 V, f = 1 MHz V_{DS} = 25 V, V_{CC} = 0 V, f = 1 MHz	C_{OSS}	 – –	 67.3 29.2	 – –	pF
Switching Characteristics NCP1129 Rise Time Fall Time NCP1126 Rise Time Fall Time	 V_{DS} = 325 V, I_{Drain} = 5.5 A, V_{GS} = 10 V, Rg = 4.7 Ω V_{DS} = 325 V, I_{Drain} = 1.8 A, V_{GS} = 10 V, Rg = 4.7 Ω	 t_r t_f t_r t_f	 – – – –	 7.6 6.0 7.2 5.9	 – – – –	ns
CURRENT SENSE						
Input Bias Current	V_{CS} = 0.8 V	I_{IB}	–	0.02	–	μA
Current Sense Voltage Threshold	V_{QCS} increasing, T_J = 25°C V_{QCS} increasing	V_{ILIM1} V_{ILIM2}	744 720	800 800	856 880	mV
Default Internal Voltage Setpoint for Frequency Foldback Trip Point	47% of V_{ILIM1}	V_{fold}	–	375	–	mV
Internal Peak Current Setpoint Freeze (31% of V_{ILIM})		V_{freeze}	–	250	–	
Cycle by Cycle Current Sense Propagation Delay	V_{QCS} dv/dt = 1 V/μs, measured from V_{QILIM1} to QDRV falling edge	$t_{CS(delay)}$	–	100	150	ns
Cycle by Cycle Leading Edge Blanking Duration		$t_{CS(LEB)}$	–	300	–	ns
INTERNAL OSCILLATOR						
Oscillation Frequency	65 kHz Version 100 kHz Version	f_{OSC1} f_{OSC2}	61 92	65 100	71 108	kHz
Maximum Duty Ratio		D_{MAX}	76	80	84	%

ELECTRICAL CHARACTERISTICS (V_{CC} = 12 V, for typical values T_J = 25°C, for min/max values, T_J is − 40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
Frequency Jittering in Percentage of f_{OSC}		f_{jitter}	–	±5	–	%
Jitter Modulation Frequency		f_{swing}	–	240	–	Hz
FEEDBACK SECTION						
Internal Pull−up Resistor		R_{up}	–	17	–	kΩ
Equivalent ac resistor from FB to GND		R_{eq}	–	15	–	kΩ
V_{FB} to Internal Current Setpoint Division Ratio		I_{ratio}	–	4	–	–
Feedback Voltage Below Which the Peak Current is Frozen		V_{freeze}	–	1	–	V
FREQUENCY FOLDBACK						
Frequency Foldback Level on the FB	47% of maximum peak current	V_{fold}	–	1.5	–	V
Transition Frequency Below Which Skip − Cycle occurs		f_{trans}	22	26	30	kHz
End of Frequency Foldback Feedback Level	$f_{SW} = f_{MIN}$	$V_{fold,end}$	–	450	–	mV
Skip − Cycle Level Voltage on The FB pin		V_{skip}	–	400	–	mV
Hysteresis on The Skip Comparator	Guaranteed by design	$V_{skip(HYS)}$	–	30	–	mV
INTERNAL SLOPE COMPENSATION						
Internal Ramp Level	T_J = 25°C		–	2.5	–	V
Internal Ramp Resistance on CS pin			–	20	–	kΩ
FAULT PROTECTION						
Soft−Start Period	Measured from 1st drive pulse to $V_{CS} = V_{ILIM}$	t_{SSTART}	–	4.0	–	ms
Overload Timer Detect Threshold on FB Pin		$V_{FB(OVL)}$	–	3.2	–	V
Overload Fault Timer	$V_{CS} = V_{ILIM}$	t_{OVLD}	TBD	200	TBD	ms
TEMPERATURE MANAGEMENT						
Temperature Shutdown	Guaranteed by Design	TSD	150	–	–	°C
Hysteresis			–	50	–	C

APPLICATION INFORMATION

Introduction

The NCP112X integrates a high−performance current−mode switcher with a 650 V MOSFET, which considerably simplifies the design of a compact and reliable switch mode power supply (SMPS). This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters and open−frame power supplies. The NCP112X brings all the necessary components normally needed in today's modern power supply designs, bringing several enhancements such as a V_{CC} OVP and an adjustable slope compensation.

- Current−mode operation with internal ramp compensation: implementing peak current mode control at a fixed 65 kHz or 100 kHz frequency, the NCP112X offers an internal ramp compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be compensated via the inclusion of a simple resistor in series with the current−sense information.
- Low startup current: reaching a low no−load standby power always represents a difficult exercise when the switcher draws a significant amount of current during start−up. A proprietary architecture in the NCP112X is guaranteed to draw less than 15 μA maximum, easing the design of low standby power adapters and enabling designs to be <100 mW at no load standby.
- EMI jittering: an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spread out the energy in a conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).
- Frequency foldback capability: a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To enhance the performance in this mode the switcher monitors the feedback pin and when it reaches a level of 1.5 V, the oscillator then starts to reduce the switching frequency as the feedback level continues to decrease. When the feedback pin reaches 1 V, the peak current setpoint is internally frozen and the frequency continues to decrease. It can go down to 26 kHz (typical) at a feedback level of ~450 mV. At this point, if power continues to drop while the feedback level drops to 400 mV, the switcher enters classical skip−cycle mode.
- Internal soft−start: a soft−start precludes the main power switch from being stressed upon start−up. In this switcher, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- Latched OVP on V_{CC}: it is sometimes required to implement a circuit protection by sensing the V_{cc} level. NCP112X does this by monitoring the V_{cc} pin. When the voltage on this pin exceeds 27.5 V typical, the pulses are immediately stopped and the part latches off. When the user cycles the V_{cc} down or the converter recovers from a brown− out event, the circuit is reset and the part enters a new start up sequence.
- Short−circuit protection: short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between the auxiliary and the power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8 V maximum peak current limit is activated, an error flag is asserted and an internal timer starts. When the fault is validated, all pulses are stopped and the switcher enters an auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. As soon as the fault disappears, the SMPS resumes operation. Please note that some versions offer an auto−recovery mode for short circuit as we just described, but versions are also available with latch off mode protection.

Start−up Sequence

The NCP112X start−up voltage is made purposely high to permit large energy storage in a small V_{CC} capacitor value. This helps to operate with a small start−up current which, together with a small V_{CC} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the switcher is extremely low, below 15 μA. The start−up resistor can therefore be connected to the bulk capacitor or directly the mains input voltage if you wish to save a few more mW.

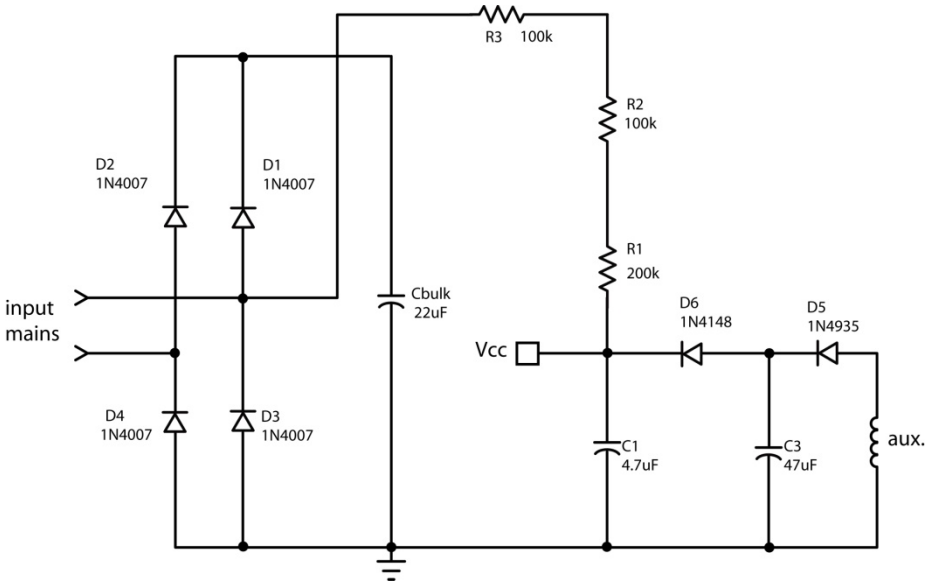


Figure 3. The Startup Resistor can be Connected to the Input Mains for Further Power Dissipation Reduction

The first step starts with the calculation of the needed V_{cc} capacitor which will supply the switcher until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{cc} capacitor must be larger than:

$$CV_{cc} \geq \frac{I_{cc}t_1}{VCC_{on} - VCC_{min}} \geq \frac{3\ m \times 10\ m}{9} \geq 3.3\ \mu F \quad \text{(eq. 1)}$$

Let us select a 4.7 μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1. The V_{cc} capacitor being known, we can now evaluate the charging current we need to bring the V_{cc} voltage from 0 to the VCC_{on} of the IC, 18 V typical. This current has to be selected to ensure a start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{VCC_{on}C_{Vcc}}{2.5} \geq \frac{18 \times 4.7\ \mu}{2.5} \geq 34\ \mu A \quad \text{(eq. 2)}$$

If we account for the 15 μA that will flow inside the switcher, then the total charging current delivered by the start−up resistor must be 49 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{CC} reaches the VCC_{on} of the switcher:

$$I_{CVcc,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 49 μA, the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{I_{CVcc,min}} \leq \frac{\frac{85 \times 1.414}{\pi} - 18}{49\ \mu} \leq 413\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{CC} capacitor. This brings a decrease in the charging current and an increase of the start−up resistor, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 400 kΩ resistor as suggested by Equation 4, the dissipated power at high line amounts to:

$$P_{Rstartup,max} = \frac{V_{ac,peak}^2}{4R_{start-up}} = \frac{\left(230 \times \sqrt{2}\right)^2}{4 \times 400\ k} = \frac{105\ k}{1.6\ Meg} = 66\ mW \quad \text{(eq. 5)}$$

Now that the first V_{cc} capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{CC} capacitor. If this ripple is too large, chances exist to touch the VCC_{min} and reset the switcher into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 3 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the V_{CC} pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the switcher without affecting the start−up time and standby power.

Triggering the SCR

The latched−state of the NCP112X is maintained via an internal thyristor (SCR). When the voltage on pin 1 exceeds the latch voltage for four consecutive clock cycles, the SCR is fired and immediately stops the output pulses. The same SCR is fired when an OVP is sensed on the V_{cc} pin. When this happens, all pulses are stopped and V_{cc} is discharged to a fix level of 7 V typically: the circuit is latched and the converter no longer delivers pulses. To maintain the

latched−state, a permanent current must be injected in the part. If too low of a current, the part de−latches and the converter resumes operation. This current is characterized to 32 μA as a minimum but we recommend including a design margin and select a value around 60 μA. The test is to latch the part and reduce the input voltage until it de−latches. If you de−latch at V_{in} = 70 V rms for a minimum voltage of 85 V rms, you are fine. If it precociously recovers, you will have to increase the start−up current, unfortunately to the detriment of standby power.

The most sensitive configuration is actually that of the half−wave connection proposed in Figure 3. As the current disappears 5 ms for a 10 ms period (50 Hz input source), the latch can potentially open at low line. If you really reduce the start−up current for a low standby power design, you must ensure enough current in the SCR in case of a faulty event. An alternate connection to the above is shown below (Figure 4):

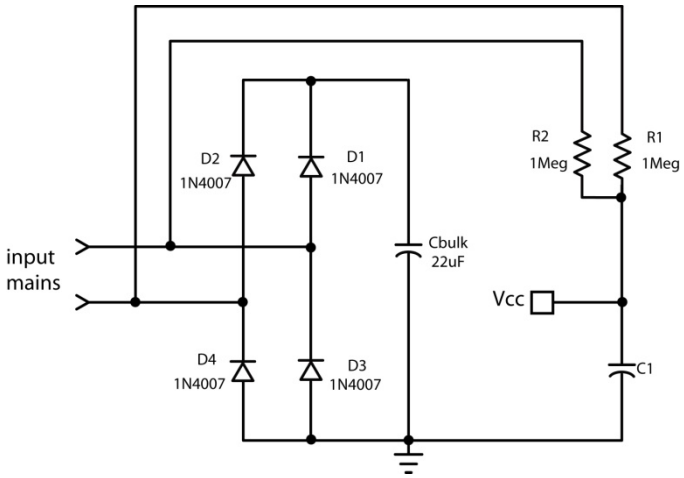


Figure 4. The Full−Wave Connection Ensures Latch Current Continuity as well as a X2−Discharge Path

In this case, the current is no longer made of 5 ms “holes” and the part can be maintained at a low input voltage. Experiments show that these 2 MΩ resistor help to maintain the latch down to less than 50 V rms, giving an excellent design margin. Standby power with this approach was also improved compared to Figure 3 solution. Please note that these resistors also ensure the discharge of the X2−capacitor up to a 0.47 μF type.

The de−latch of the SCR occurs when a) the injected current in the V_{cc} pin falls below the minimum stated in the data−sheet (32 μA at room temp) or when the part senses a brown−out recovery.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This switcher implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold}, set around 1.5 V. At this point, the oscillator turns into a Voltage−Controlled Oscillator and reduces its switching frequency. The peak current setpoint is following the feedback pin until its level reaches 1 V. Below this value, the peak current freezes to V_{freeze}/4 (250 mV or ≈31% of the maximum 0.8 V setpoint) and the only way to further reduce the transmitted power is to diminish the operating frequency down to 26 kHz. This value is reached at a voltage feedback level of 450 mV typically. Below this point, if the output power continues to decrease, the part enters skip cycle for the best noise−free performance in no−load conditions. Figure 5 depicts the adopted scheme for the part.

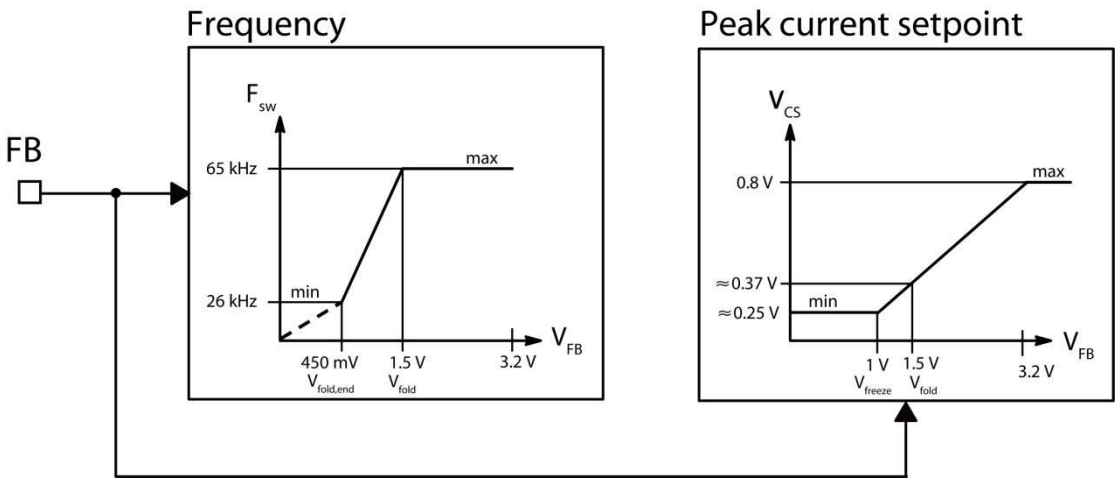


Figure 5. By Observing the Voltage on the Feedback Pin, the Switcher Reduces its Switching Frequency for an Improved Performance at Light Load

Auto−Recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than 200 ms, the driving pulses are stopped and V_{CC} falls down as the auxiliary pulses are missing. When it crosses $VCC_{(min)}$, the switcher consumption is down to a few μA and the V_{CC} slowly builds up again thanks to the resistive starting network. When V_{CC} reaches VCC_{ON}, the switcher purposely ignores the re−start and waits for another V_{CC} cycle: this is the so−called double hiccup. By lowering the duty−ratio in fault condition, it naturally reduces the average input power and the rms current in the output cable. Illustration of such principle appears in Figure 6. Please note that soft−start is activated upon re−start attempt.

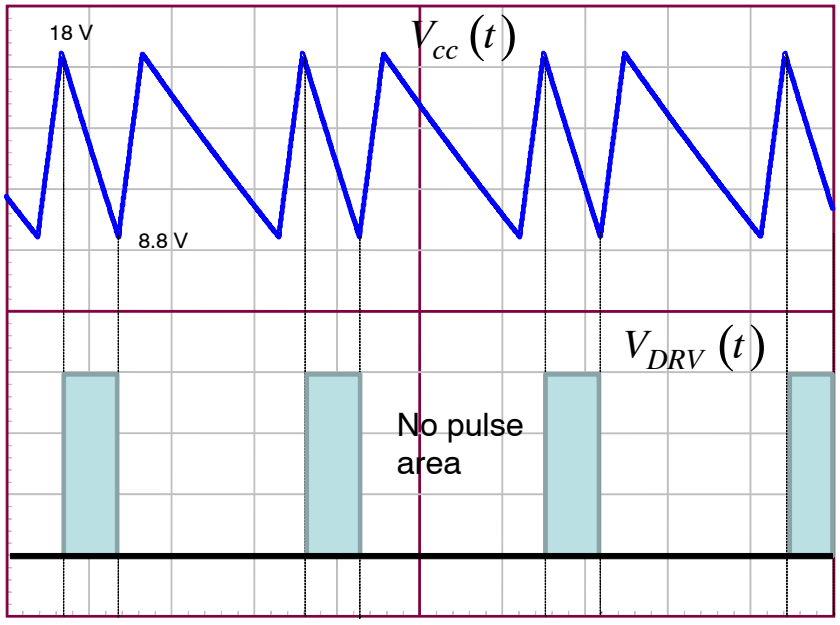


Figure 6. An Auto−Recovery Hiccup Mode is Entered in Case a Faulty Event Longer than 100 ms is Acknowledged by the Switcher

Ramp Compensation

The NCP112X includes an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude is around 2.5 V at the maximum authorized duty−ratio. Ramp compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−ratio greater than 50%. To lower the current

loop gain, one usually mixes between 50% and 100% of the inductor downslope with the current−sense signal. Figure 7 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off−time.

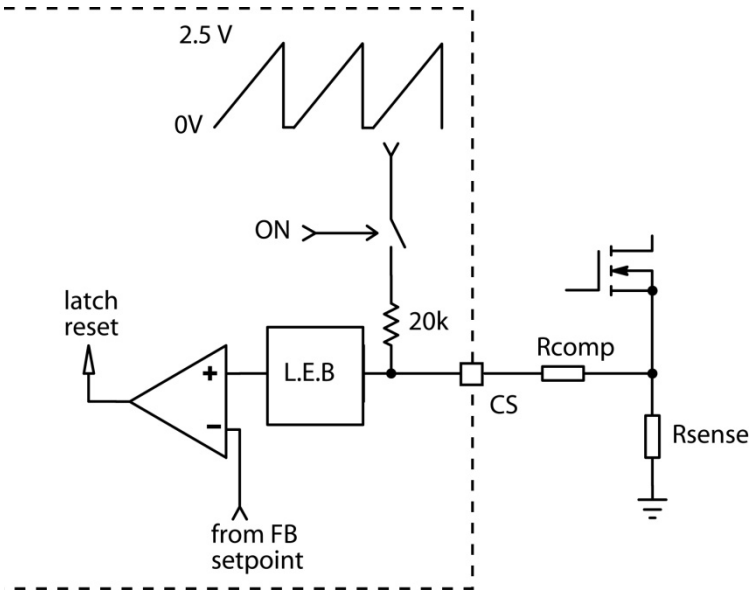


Figure 7. Inserting a Resistor in Series with the Current Sense Information Brings Slope Compensation and Stabilizes the Converter in CCM Operation

In the NCP112X switcher, the oscillator ramp exhibits a 2.5 V swing reached at a 80% duty−ratio. If the clock operates at a 65 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max}T_{sw}} = \frac{2.5}{0.8 \times 15\,\mu} = 208\ \text{kV/s or 208 mV/}\mu\text{s} \quad \text{(eq. 6)}$$

In our flyback design, let's assume that our primary inductance L_p is 770 μH, and the SMPS delivers 19 V with a N_p:N_s turns ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_p = \frac{\left(V_{out} + V_f\right)\frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{770\,\mu} = 103\ \text{kA/s} \quad \text{(eq. 7)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 103\text{k} \times 0.33 = 34\text{kV/s or } 34\text{mV/}\mu\text{s} \quad \text{(eq. 8)}$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is 17 mV/μs. Our internal compensation being of 208 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor is:

$$\text{divratio} = \frac{17\ \text{m}}{208\ \text{m}} = 0.082 \quad \text{(eq. 9)}$$

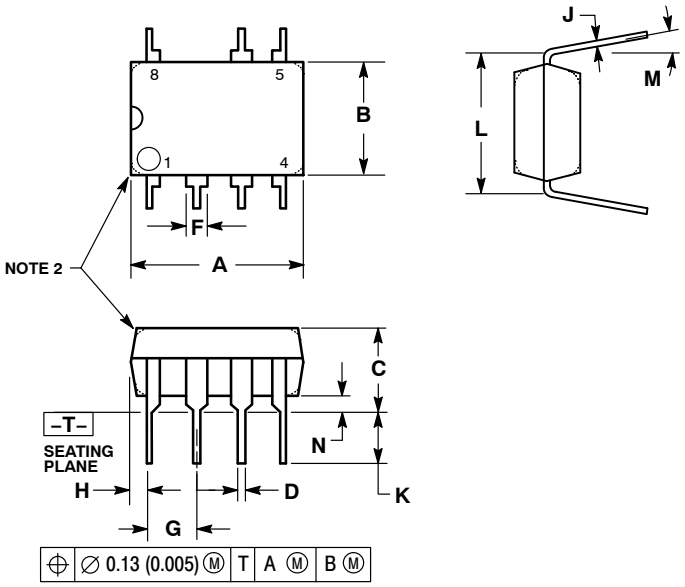
The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}\text{divratio} = 20\ \text{k} \times 0.082 \approx 1.6\ \text{k}\Omega \quad \text{(eq. 10)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small 100 pF capacitor, from the current sense pin to the switcher ground for improved noise immunity. Please make sure both components are located very close to the switcher.

PACKAGE DIMENSIONS

7−LEAD PDIP
CASE 626B
ISSUE A



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.

	MILLIMETERS	
DIM	MIN	MAX
A	9.40	10.16
B	6.10	6.60
C	3.94	4.45
D	0.38	0.51
F	1.02	1.78
G	2.54 BSC	
H	0.76	1.27
J	0.20	0.30
K	2.92	3.43
L	7.62 BSC	
M	−−−	10 °
N	0.76	1.01

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