General Description

The 844441 is a low jitter, high performance clock generator and a member of the FemtoClock® family of silicon timing products. The 844441 is designed for use in applications using the SAS and SATA interconnect. The 844441 uses an external, 25MHz, parallel resonant crystal to generate four selectable output frequencies: 75MHz, 100MHz, 150MHz, and 300MHz. This silicon based approach provides excellent frequency stability and reliability. The 844441 features down and center spread spectrum (SSC) clocking techniques.

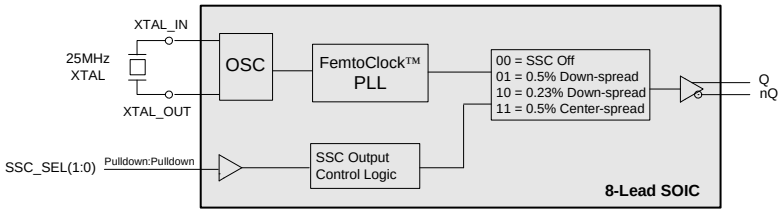
Applications

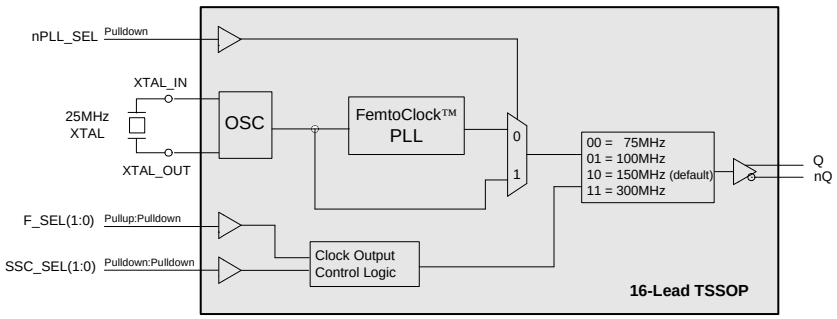
- SAS/SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and TapeDrives
- Disk Storage Enterprise

Features

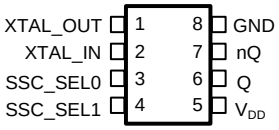
- Designed for use in SAS, SAS-2, and SATA systems
- Center (±0.17%) Spread Spectrum Clocking (SSC)
- Down (-0.23% or -0.5%) SSC
- Better frequency stability than SAW oscillators
- One differential 2.5V LVDS output
- Crystal oscillator interface designed for 25MHz (C_L = 12pF) frequency
- External fundamental crystal frequency ensures high reliability and low aging
- Selectable output frequencies: 75MHz, 100MHz, 150MHz, 300MHz
- Output frequency is tunable with external capacitors
- RMS phase jitter @ 100MHz, using a 25MHz crystal (12kHz – 20MHz): 1.1936ps (typical)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagrams

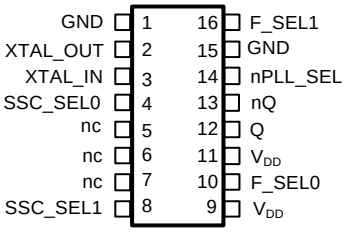




Pin Assignment



844441
8-Lead SOIC, 3.90mm x 4.90mm Package



844441
16-Lead TSSOP, 4.4mm x 5.0mm Package

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Name	Type		Description
XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
SSC_SEL0, SSC_SEL1	Input	Pulldown	SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.
F_SEL0	Input	Pulldown	Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.
F_SEL1	Input	Pullup	Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.
nPLL_SEL	Input	Pulldown	PLL Bypass pin. LVCMOS/LVTTL interface levels.
Q, nQ	Output		Differential clock outputs. LVDS interface levels.
GND	Power		Power supply ground.
V_{DD}	Power		Power supply pin.
nc	Unused		No connect.

NOTE: *Pullup/Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	nPLL_SEL, F_SEL[1:0], SSC_SEL[1:0]		4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Tables

Table 3A. SSC_SEL[1:0] Function Table

Inputs		Mode
SSC_SEL1	SSC_SEL0	
0 (default)	0 (default)	SSC Off
0	1	0.5% Down-spread
1	0	0.23% Down-spread
1	1	0.34% Center-spread

Table 3B. F_SEL[1:0] Function Table

Inputs		Output Frequency (MHz)
F_SEL1	F_SEL0	
0	0	75
0	1	100
1 (default)	0 (default)	150
1	1	300

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA} 16 Lead TSSOP 8 Lead SOIC	 81.2°C/W (0 mps) 96.0°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				73	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.7	V
I_{IH}	Input High Current	F_SEL1	V_{DD} = V_{IN} = 2.5V			5	µA
		SSC_SEL[0:1], F_SEL0, nPLL_SEL	V_{DD} = V_{IN} = 2.5V			150	µA
I_{IL}	Input Low Current	F_SEL1	V_{DD} = 2.5V, V_{IN} = 0V	-150			µA
		SSC_SEL[0:1], F_SEL0, nPLL_SEL	V_{DD} = 2.5V, V_{IN} = 0V	-5			µA

Table 4C. LVDS DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200		454	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1		1.375	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 4D. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ohm
Shunt Capacitance				7	pF
Load Capacitance (C_L)			12		pF

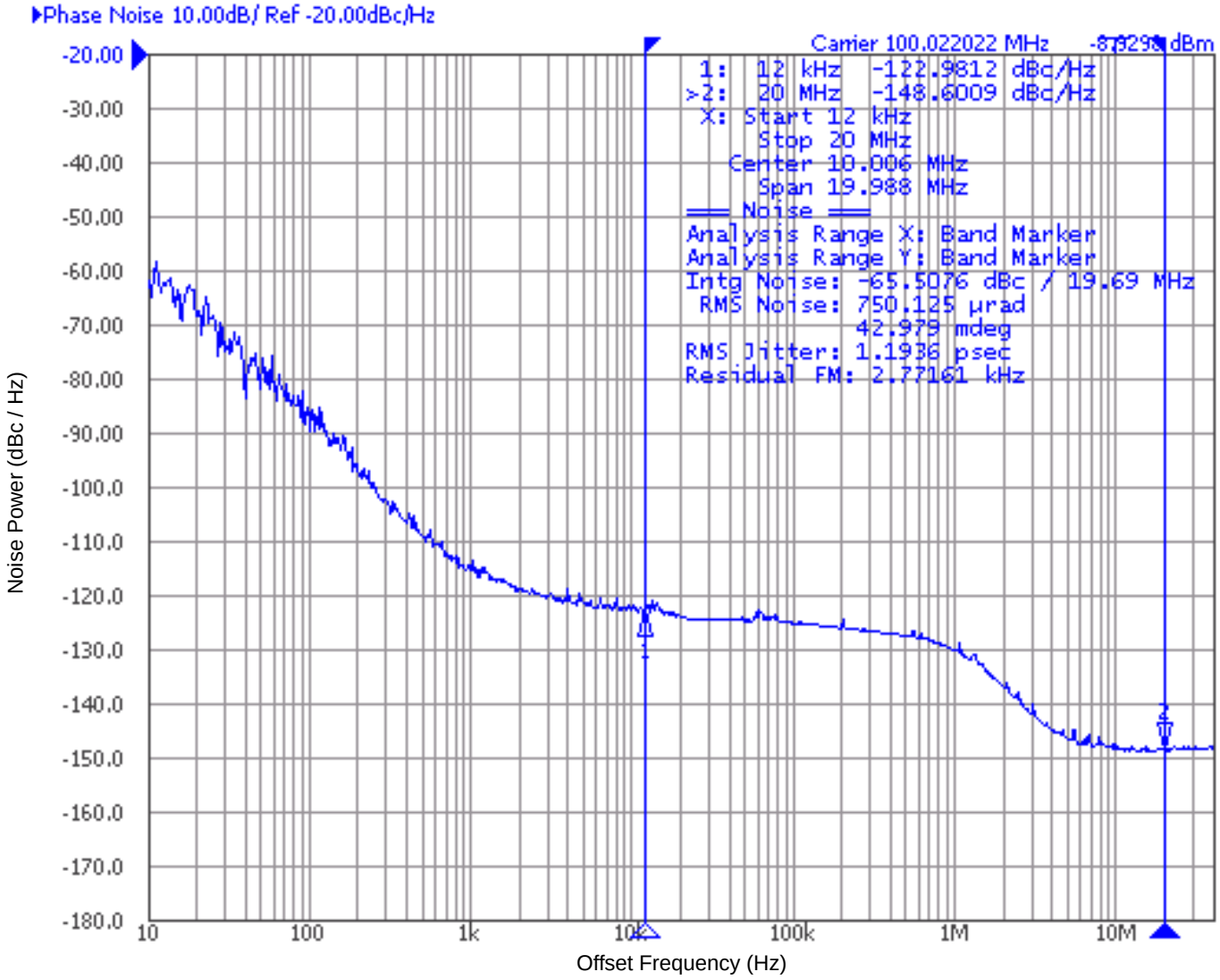
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = -40°C to 85°C

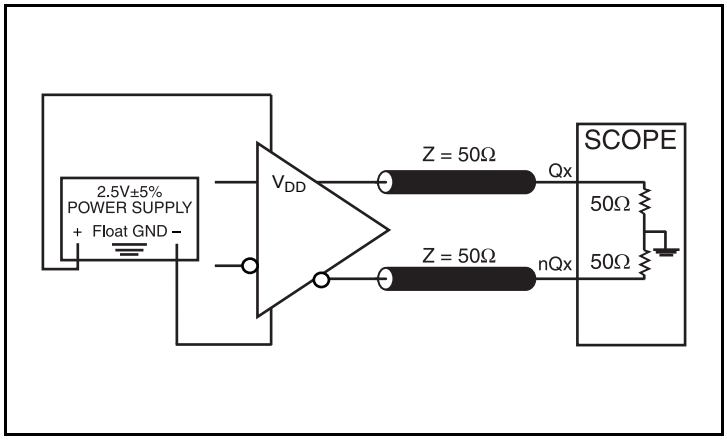
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	F_SEL(1:0) = 00		75		MHz
		F_SEL(1:0) = 01		100		MHz
		F_SEL(1:0) = 10		150		MHz
		F_SEL(1:0) = 11		300		MHz
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 1	75MHz, Integration Range: 12kHz – 20MHz		1.19602		ps
		100MHz, Integration Range: 12kHz – 20MHz		1.1936		ps
		150MHz, Integration Range: 12kHz – 20MHz		1.22743		ps
		300MHz, Integration Range: 12kHz – 20MHz		1.15011		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		400	ps
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using a 25MHz, 12pF quartz crystal.
NOTE 1: Please refer to the Phase Noise plot.

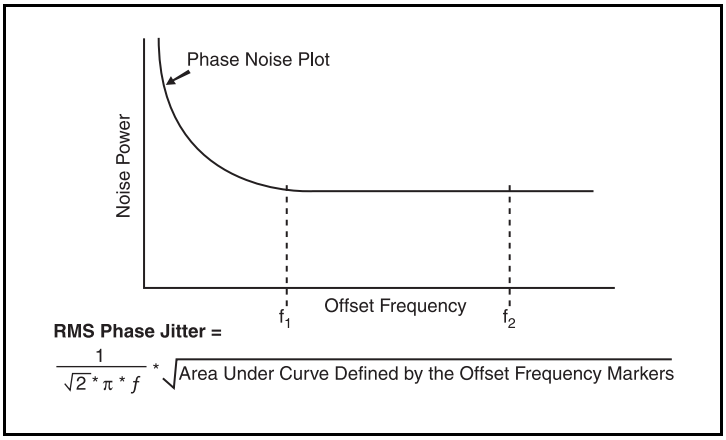
Typical Phase Noise at 100MHz



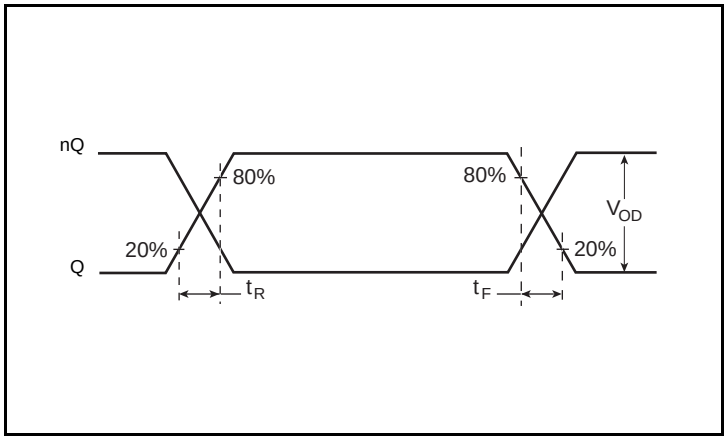
Parameter Measurement Information



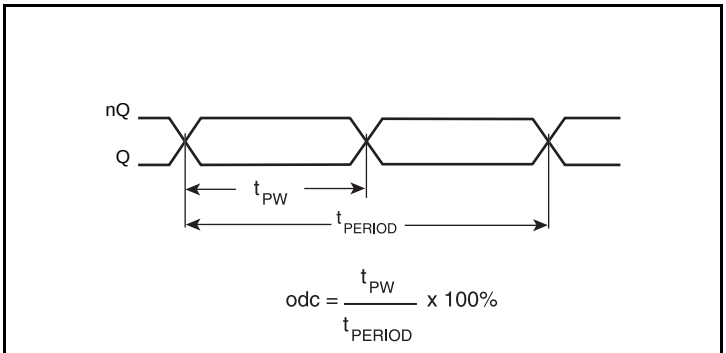
2.5V LVDS Output Load Test Circuit



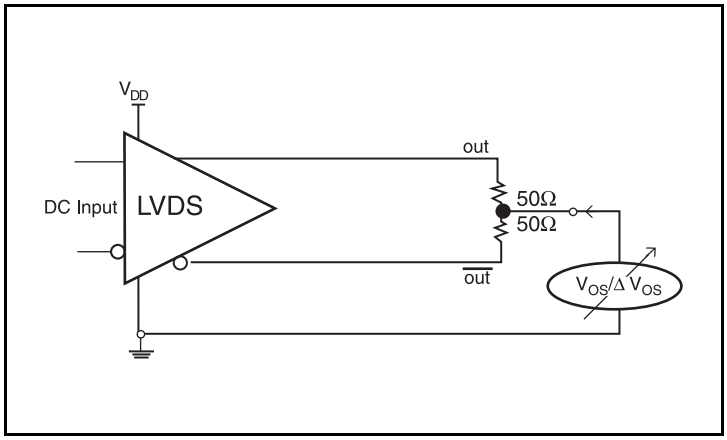
RMS Phase Jitter



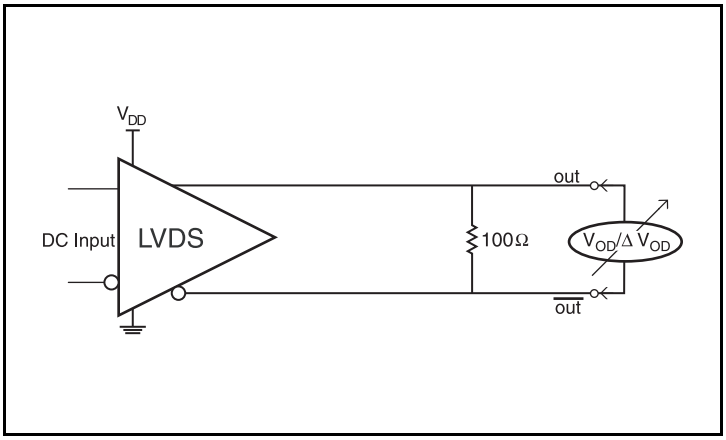
Output Rise/Fall Time



Output Duty Cycle/Pulse Width/Period



Offset Voltage Setup



Differential Output Voltage Setup

Application Information

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

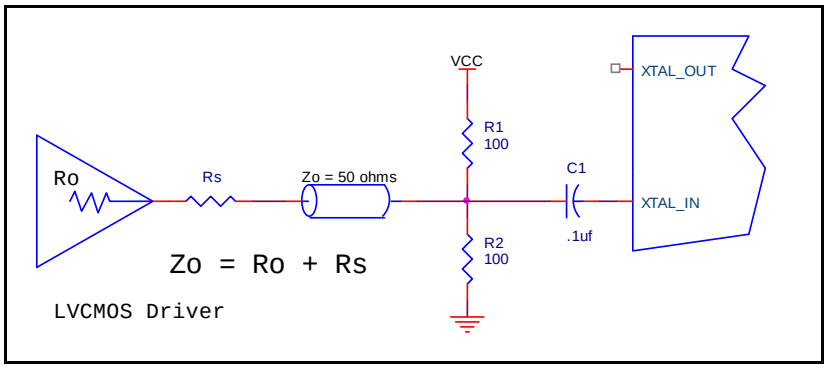


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

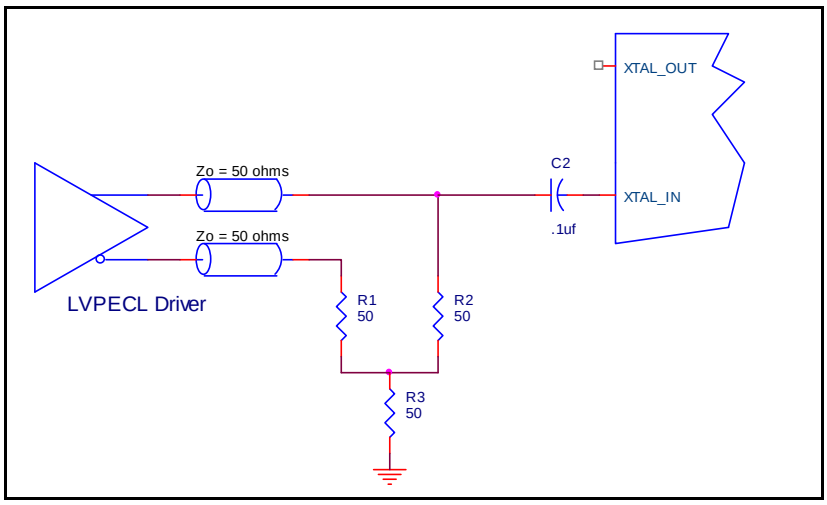


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 2A* can be used with either type of output structure. *Figure 2B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

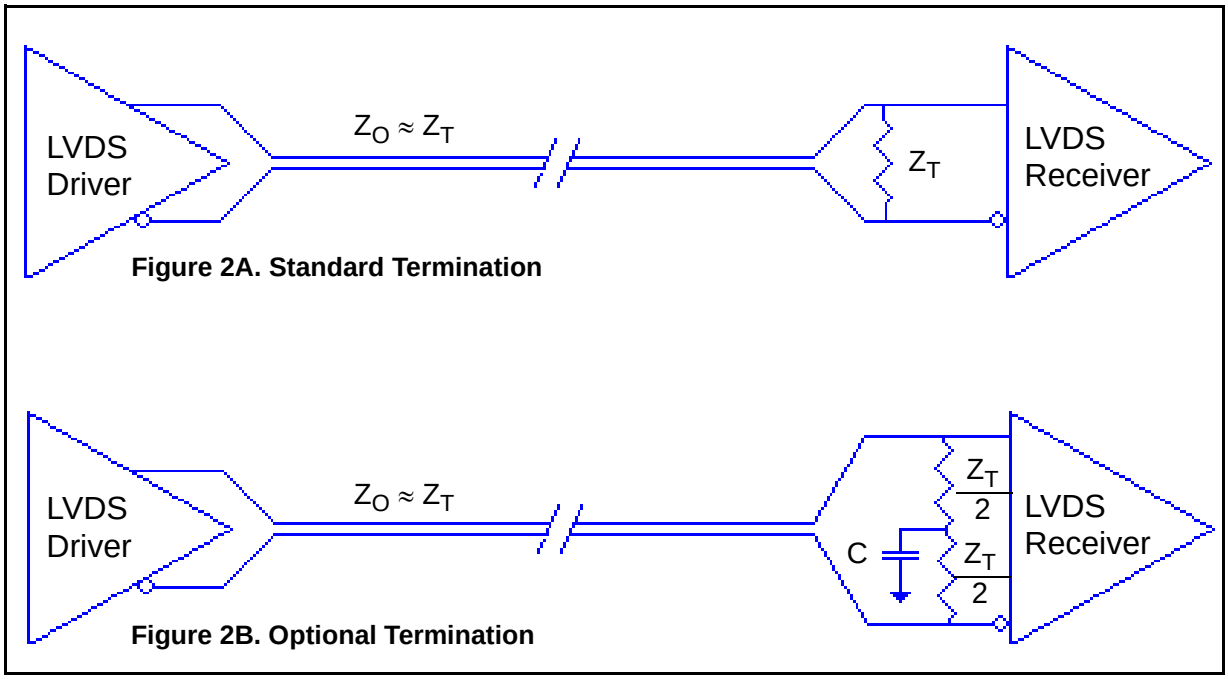


Figure 2A. Standard Termination

Figure 2B. Optional Termination

LVDS Termination

Schematic Example

Figures 3A and 3B are example 844441 application schematics for either the 8 pin M package or the 16 pin G package. The schematic examples focus on functional connections and are not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example, the device is operated at V_{DD} = 2.5V. A 12pF parallel resonant 25MHz crystal is used with tuning capacitors C1 = C2 =14pF, which are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the Xtal_In and Xtal_Out pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. In circuit board design, return the capacitors to ground through a single point contact close to the package. Two examples of terminations for LVDS receivers without built-in termination are shown in this schematic.

In order to achieve the best possible filtering, it is recommended that the placement of the power filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

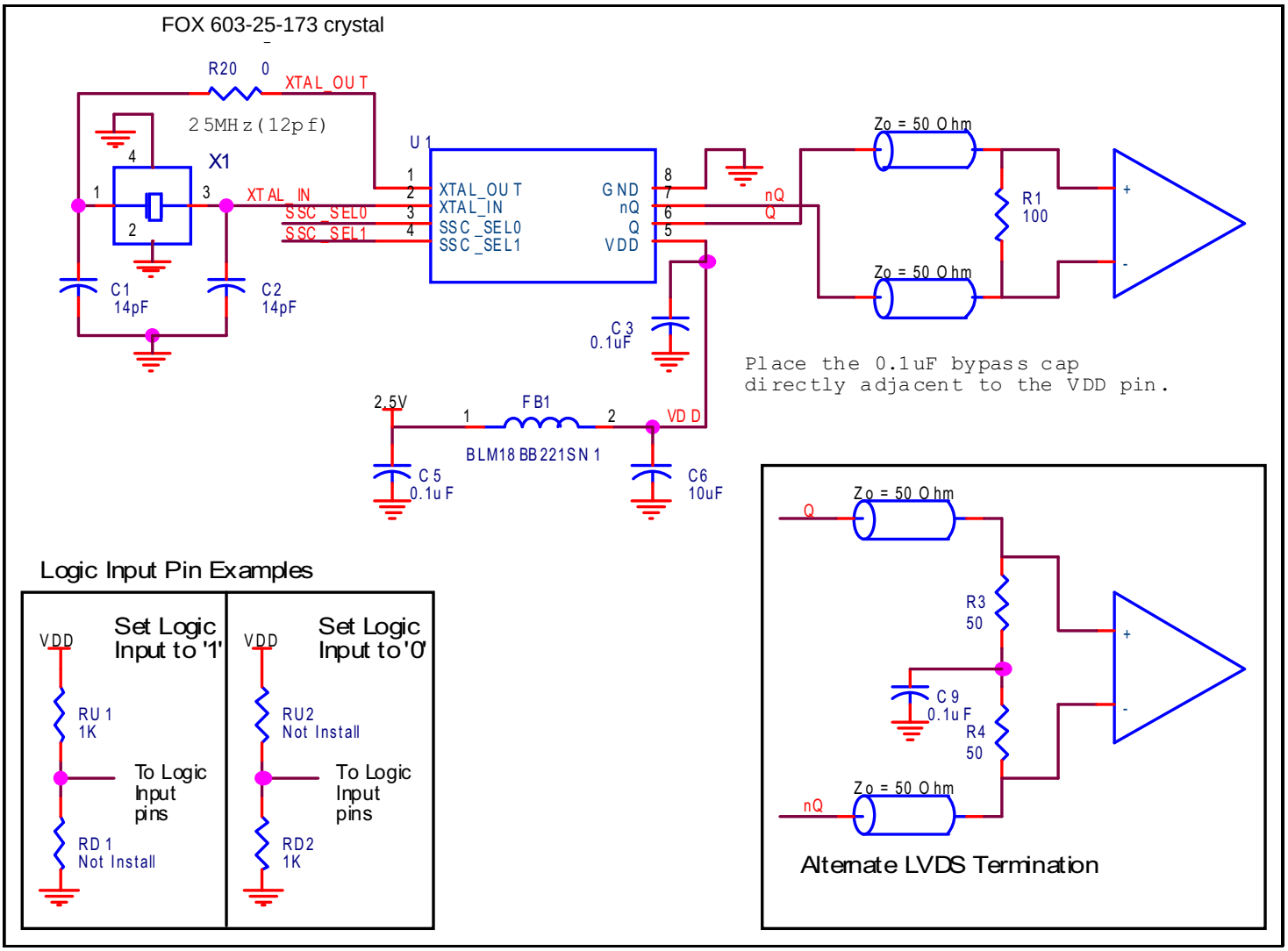


Figure 3A. 844441 Schematic Example

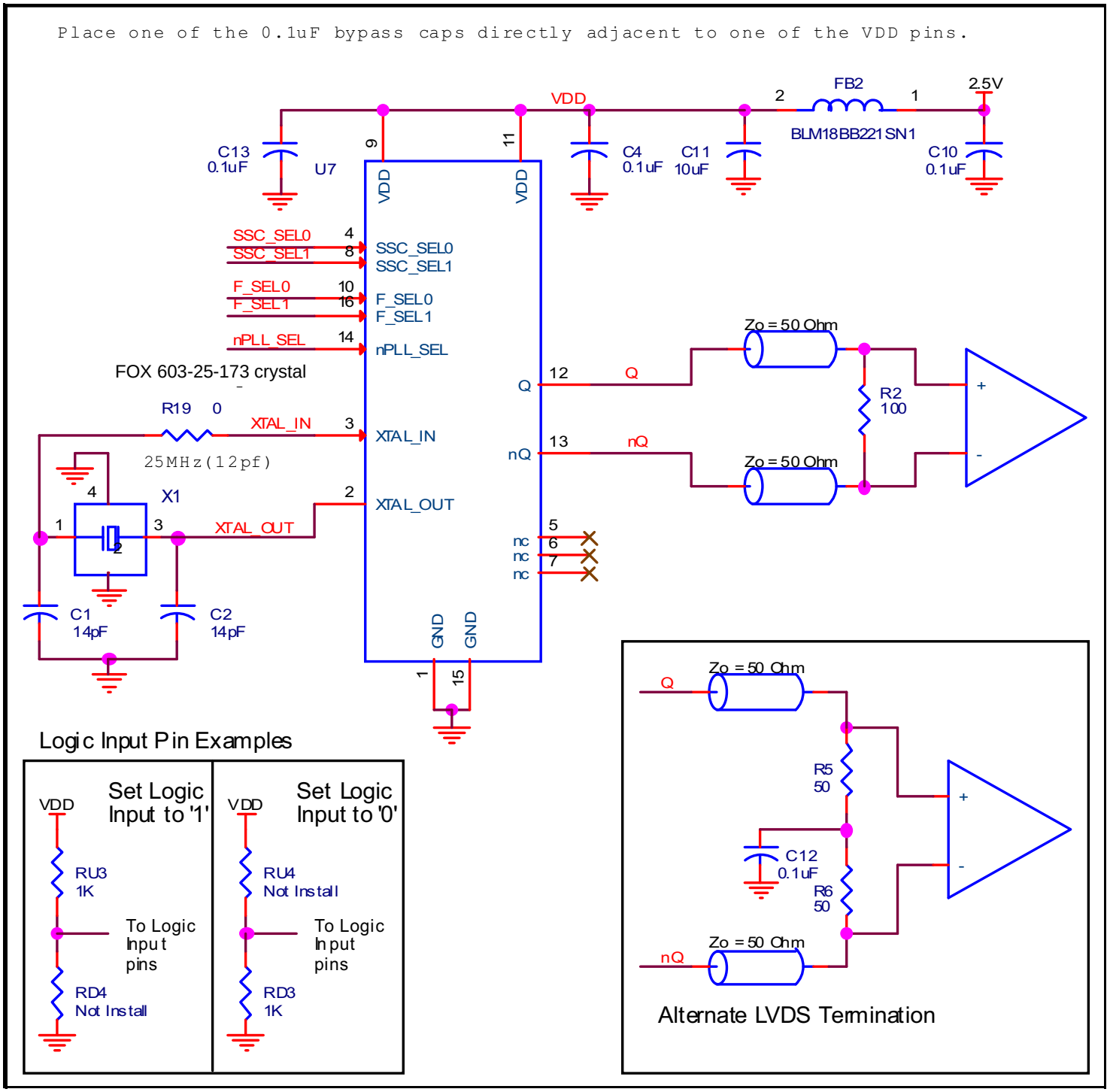


Figure 3B. 844441 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 844441.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844441 is the sum of the core power plus the power dissipated due to loading.
The following is the power dissipation for V_{DD} = 2.5V + 5% = 2.625V, which gives worst case results.

Total Power $_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 2.625V * 73mA = **191.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 6B below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.192W * 96°C/W = 103.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the supply voltage, air flow and the type of board (multi-layer).

Table 6A. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Table 6B. Thermal Resistance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} vs. Air Flow			
Linear Feet per Second	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Reliability Information

Table 7A. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Table 7B. θ_{JA} vs. Air Flow Table for a 8 Lead SOIC

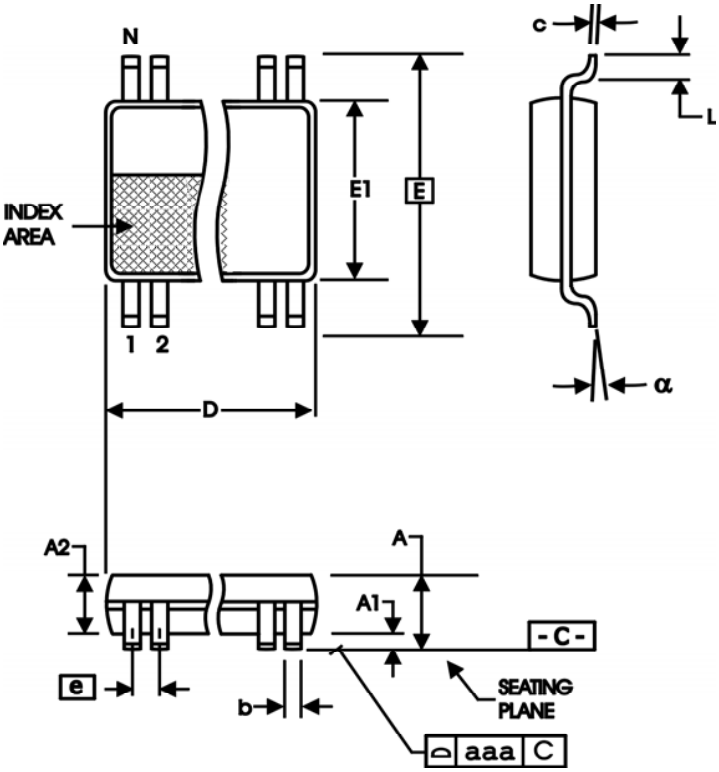
θ_{JA} vs. Air Flow			
Linear Feet per Second	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	96°C/W	87°C/W	82°C/W

Transistor Count

The transistor count for 844441 is: 3374

Package Outline and Package Dimensions

Package Outline - G Suffix for 16-Lead TSSOP



Package Outline - M Suffix for 8 Lead SOIC

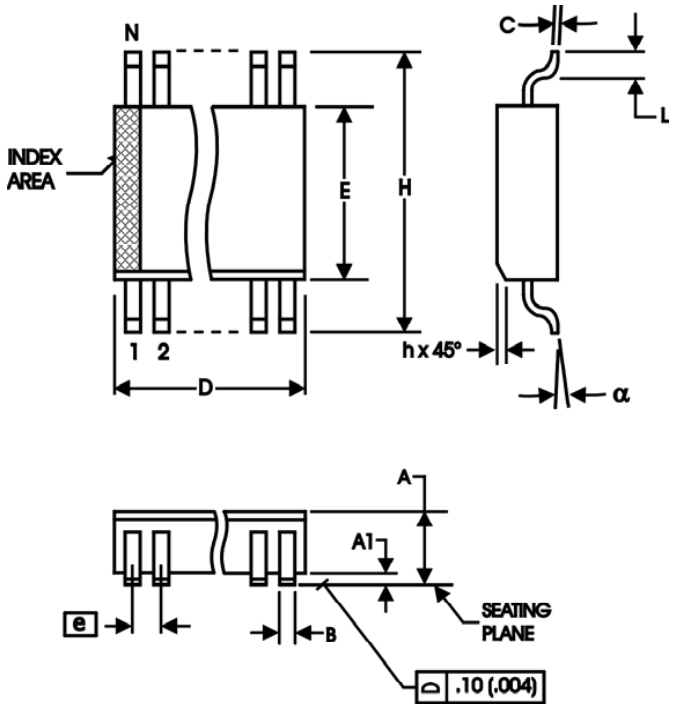


Table 8A. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8B. Package Dimensions for 8 Lead SOIC

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Output Frequency (MHz)	Package	Shipping Packaging	Temperature
844441DGILF	44441DIL	75, 100, 150, 300	16 Lead TSSOP, Lead-Free	Tube	-40°C to 85°C
844441DGILFT	44441DIL	75, 100, 150, 300	16 Lead TSSOP, Lead-Free	Tape & Reel	-40°C to 85°C
844441DMI-75LF	441DI75L	75	8 Lead SOIC, Lead-Free	Tube	-40°C to 85°C
844441DMI-75LFT	441DI75L	75	8 Lead SOIC, Lead-Free	Tape & Reel	-40°C to 85°C
844441DMI-100LF	41DI100L	100	8 Lead SOIC, Lead-Free	Tube	-40°C to 85°C
844441DMI-100LFT	41DI100L	100	8 Lead SOIC, Lead-Free	Tape & Reel	-40°C to 85°C
844441DMI-150LF	41DI150L	150	8 Lead SOIC, Lead-Free	Tube	-40°C to 85°C
844441DMI-150LFT	41DI150L	150	8 Lead SOIC, Lead-Free	Tape & Reel	-40°C to 85°C
844441DMI-300LF	41DI300L	300	8 Lead SOIC, Lead-Free	Tube	-40°C to 85°C
844441DMI-300LFT	41DI300L	300	8 Lead SOIC, Lead-Free	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T4D T5	1 4 4 9 - 10	Features Section, Crystal Oscillator bullet, added additional crystal recommendation. Crystal Characteristics Table - added crystal recommendation note. AC Characteristics Table - added additional crystal recommendation to 2nd note. Application Schematics - in schematics, added additional crystal recommendation. Deleted part number prefix/suffix throughout the datasheet. Updated datasheet header/footer.	5/5/15
C		9 - 10	Updated Application Schematics.	7/31/15
D		1	PDN #CQ-15-04 Product Discontinuance Notice – Last Time buy Expires on August 14, 2016.	08/21/15
E		9 - 10	The 844441 datasheet is obsolete per PDN #CQ-15-04. Application Schematic, IDT crystal part number was replaced by FOX part number.	11/2/16

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
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