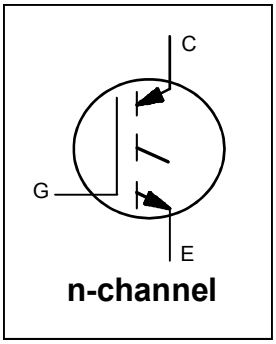
IRG7CH54K10EF

INSULATED GATE BIPOLAR TRANSISTOR

V_{CES} = 1200V
$I_{C(Nominal)}$ = 50A
$T_{J(max)}$ = 175°C
$V_{CE(on)}$ typ = 1.9V @ I_C= 50A



n-channel

Applications

- Medium Power Drives
- UPS
- HEV Inverter
- Welding
- Induction Heating

G	C	E
Gate	Collector	Emitter

Features	→	Benefits
Low $V_{CE(ON)}$ and switching Losses		High efficiency in a wide range of applications and switching frequencies
Square RBSOA and Maximum Junction Temperature 175°C		Improved Reliability due to rugged hard switching performance and higher power capability
Positive $V_{CE\ (ON)}$ Temperature Coefficient		Excellent current sharing in parallel operation

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG7CH54K10EF	Die on Film	Wafer	1	IRG7CH54K10EF

Mechanical Parameter

Die Size	7.55 x 7.55	mm^2
Minimum Street Width	75	µm
Emiter Pad Size (Included Gate Pad)	See Die Drawing	mm^2
Gate Pad Size	0.509 x 0.503	
Area Total / Active	57/ 40.1	
Thickness	140	µm
Wafer Size	200	mm
Notch Position	0	Degrees
Maximum-Possible Chips per Wafer	465 pcs.	
Passivation Front side	Silicon Nitride	
Front Metal	Al, Si (4µm)	
Backside Metal	Al (0.1µm), Ti (0.1µm), Ni (0.4µm), Ag (0.6µm)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, T_J=25°C	1200	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ④	200	A
V_{GE}	Gate Emitter Voltage	± 30	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	°C

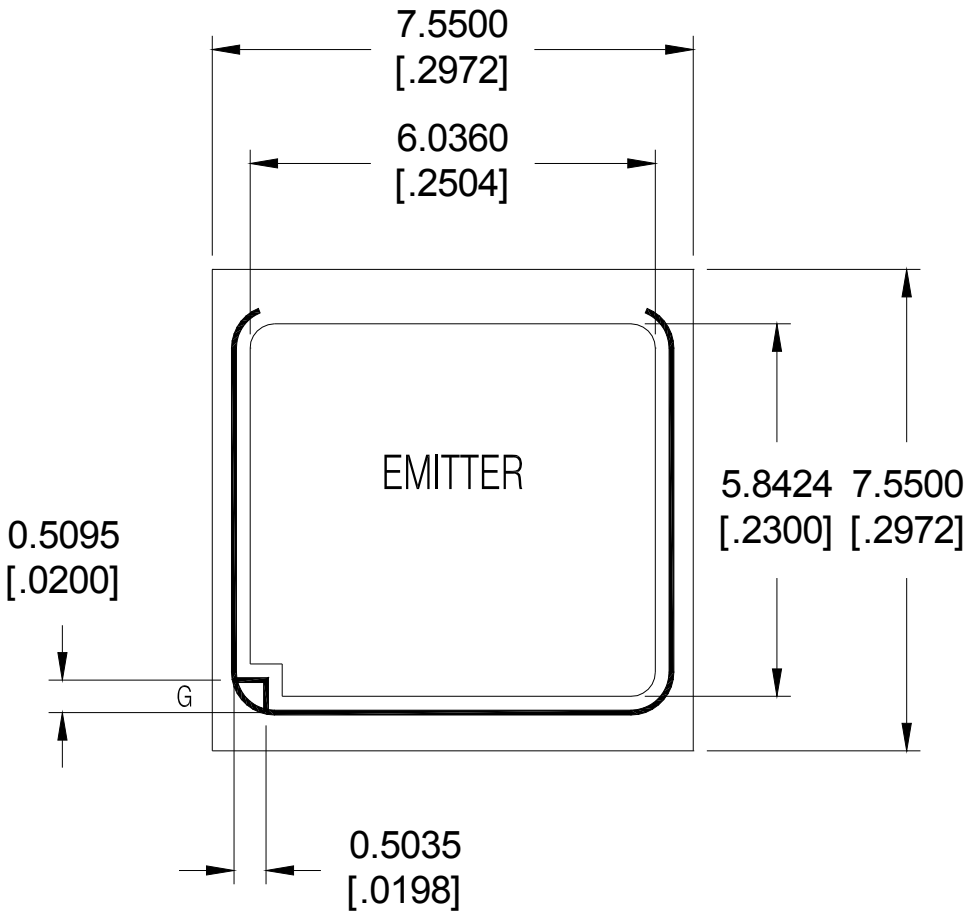
Static Characteristics (Tested on wafers) . T_J=25°C

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 250µA ⑤
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.25	1.5		V_{GE} = 15V, I_C = 10A, T_J = 25°C
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	5.0	—	7.5		I_C = 2.4mA , V_{GE} = V_{CE}
I_{CES}	Zero Gate Voltage Collector Current	—	1.0	25	µA	V_{CE} = 1200V, V_{GE} = 0V
I_{GES}	Gate Emitter Leakage Current	—	—	± 200	nA	V_{CE} = 0V, V_{GE} = ±30V

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.9	2.3	V	V_{GE} = 15V, I_C = 50A , T_J = 25°C
		—	2.5	—		V_{GE} = 15V, I_C = 50A , T_J = 175°C
SCSOA	Short Circuit Safe Operating Area	10	—	—	µs	V_{GE}=15V, V_{CC}=600V, ② R_G=5Ω, V_P ≤1200V,T_J=150°C
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 200A V_{CC} = 960V, Vp ≤1200V Rg = 5Ω, V_{GE} = +20V to 0V
C_{iss}	Input Capacitance	—	6240	—	pF	V_{GE} = 0V
C_{oss}	Output Capacitance	—	230	—		V_{CE} = 30V
C_{rss}	Reverse Transfer Capacitance	—	150	—		f = 1.0MHz
Q_g	Total Gate Charge (turn-on)	—	290	—	nC	I_C = 50A ⑥
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	60	—		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	130	—		V_{CC} = 600V

	Parameter	Min.	Typ.	Max.	Units	Conditions ③
$t_{d(on)}$	Turn-On delay time	—	75	—	ns	I_C = 50A, V_{CC} = 600V
t_r	Rise time	—	60	—		R_G = 5Ω, V_{GE}=15V, L=200µH
$t_{d(off)}$	Turn-Off delay time	—	305	—		T_J = 25°C
t_f	Fall time	—	55	—		
$t_{d(on)}$	Turn-On delay time	—	70	—		I_C = 50A, V_{CC} = 600V
t_r	Rise time	—	60	—		R_G = 5Ω, V_{GE}=15V, L= 200µH
$t_{d(off)}$	Turn-Off delay time	—	345	—		T_J = 175°C
t_f	Fall time	—	185	—		

Die Drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: MILLIMETERS
3. LETTER DESIGNATION:
   S = SOURCE SK = SOURCE KELVIN E = EMITTER
   G = GATE IS = CURRENTSENSE
4. DIMENSIONAL TOLERANCES:

BONDING PADS:	< 0.635	TOLERANCE = +/- 0.013
WIDTH	< [.0250]	TOLERANCE = +/- [.0005]
&	> 0.635	TOLERANCE = +/- 0.025
LENGTH	> [.0250]	TOLERANCE = +/- [.0010]
OVERALL DIE:	< 1.270	TOLERANCE = +/- 0.102
WIDTH	< [.050]	TOLERANCE = +/- [.004]
&	> 1.270	TOLERANCE = +/- 0.203
LENGTH	> [.050]	TOLERANCE = +/- [.008]

5. DIE THICKNESS = 0.140 [.0055] TOL: = 0.007 [.0003]

REFERENCE: IRG7CH54K10B

Notes:

① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.
② Not subject to production test- Verified by design / characterization.
③ Values influenced by parasitic L and C in measurement.
④ V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 19µH, R_G = 5Ω.
⑤ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely
⑥ Die Level Characterization.

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

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Further Information

For further information please contact your local IR Sales office or email your enquiry to http://die.irf.com

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.

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