# 6 Channel DC/DC Converters

## General Description

The RT9911 is a complete power-supply solution for digital still cameras and other hand-held devices. It integrates one selectable Boost/Buck DC/DC converter, one high efficiency step-down DC/DC converter, one high efficiency main step-up converter, one PWM converter for CCD positive voltage, one inverter for CCD negative voltage and one white LED driver for LCD backlight. The RT9911 is targeted for applications that use either two or three primary cells or a single lithium-ion battery.

RT9911 is available in VQFN-40L 6x6. Each DC-DC converter has independent shutdown input.

## Ordering Information

RT9911 □□

Package Type
QV : VQFN-40L 6x6 (V-Type)
Lead Plating System
P : Pb Free
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

## Applications

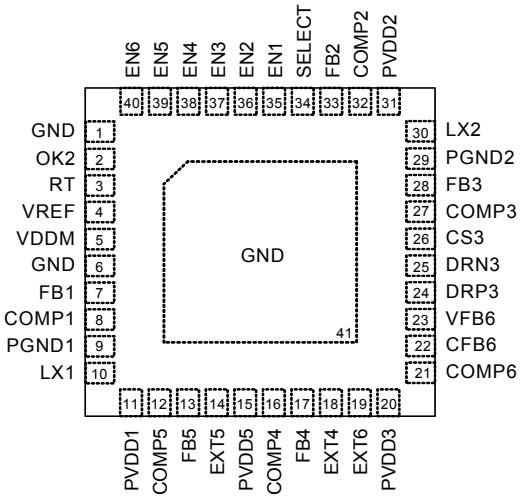
- Digital Still Camera
- PDA
- Protable Device

## Features

- **1.6V to 5.5V Battery Input Voltage Range**
- **Synchronous Boost/Buck Selectable DC/DC Converter**
  - **Internal Switches**
  - **Up to 95% Efficiency**
- **Syn-Buck DC/DC Converters**
  - **0.8V to 5.5V Adjustable Output Voltage**
  - **Up to 95% Efficiency**
  - **100%(MAX) Duty Cycle**
  - **Internal Switches**
- **Main Boost DC/DC Converter**
  - **Adjustable Output Voltage**
  - **Up to 97% Efficiency**
- **PWM Converter for CCD Positive Voltage**
- **Inverter for CCD Negative Voltage**
- **White LED Driver for LCD Panel Backlight**
- **Up to 1.4MHz Adjustable Switching Frequency**
- **1μA Supply Current in Shutdown Mode**
- **External Compensation Network for all Converters**
- **Independent Enable Pin to Shutdown Each Channel.**
- **40-Lead VQFN Package**
- **RoHS Compliant and 100% Lead (Pb)-Free**

## Pin Configurations

(TOP VIEW)




VQFN-40L 6x6

## Typical Application Circuit

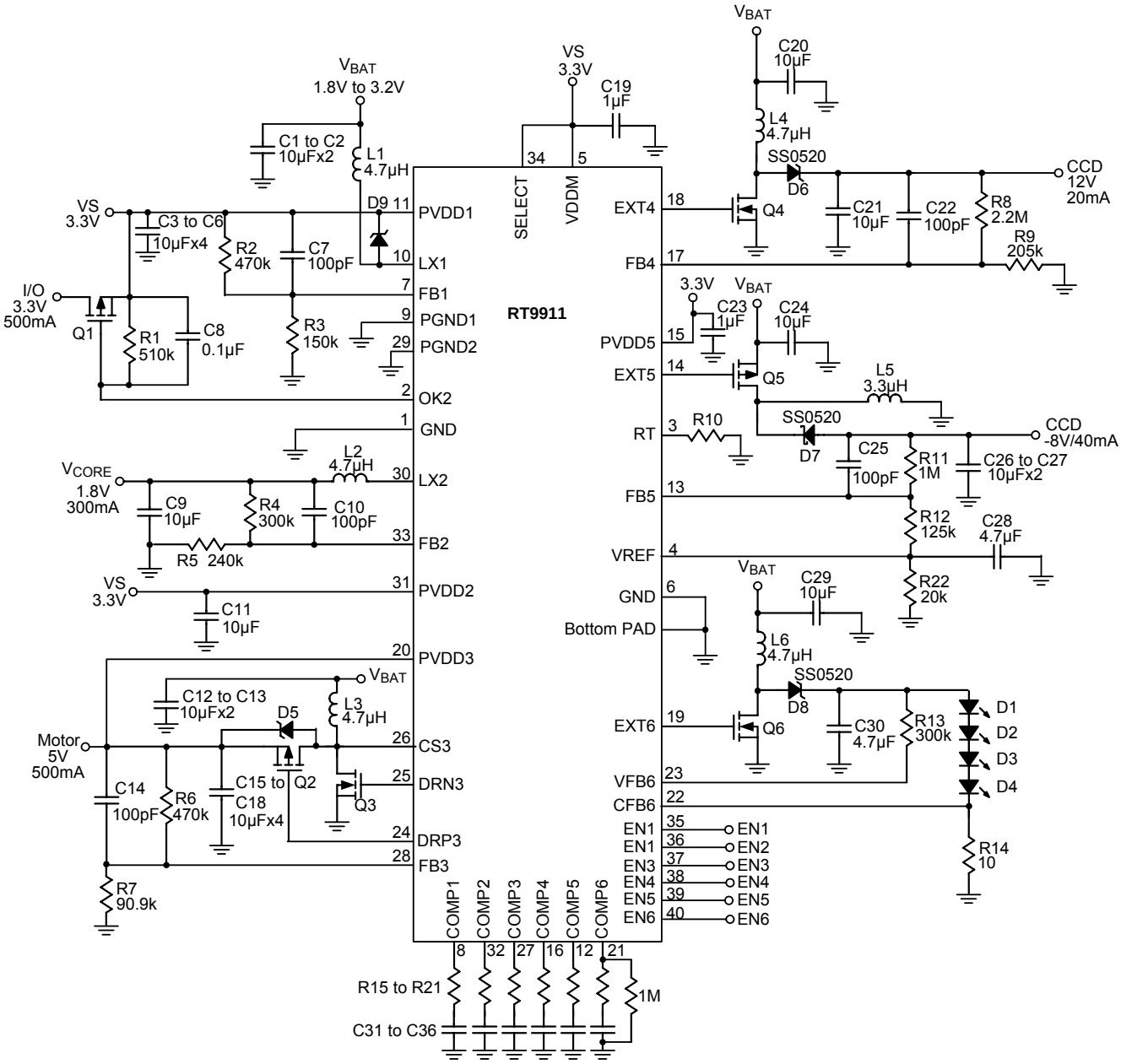



Figure 1. Application Circuit for 2-Cells Battery Supply

Note :

- Bottom pad is GND pad, can be short to pin 6 (GND).
- Please remove Q2 when use Async Boost and remove D5 when use Sync Boost.

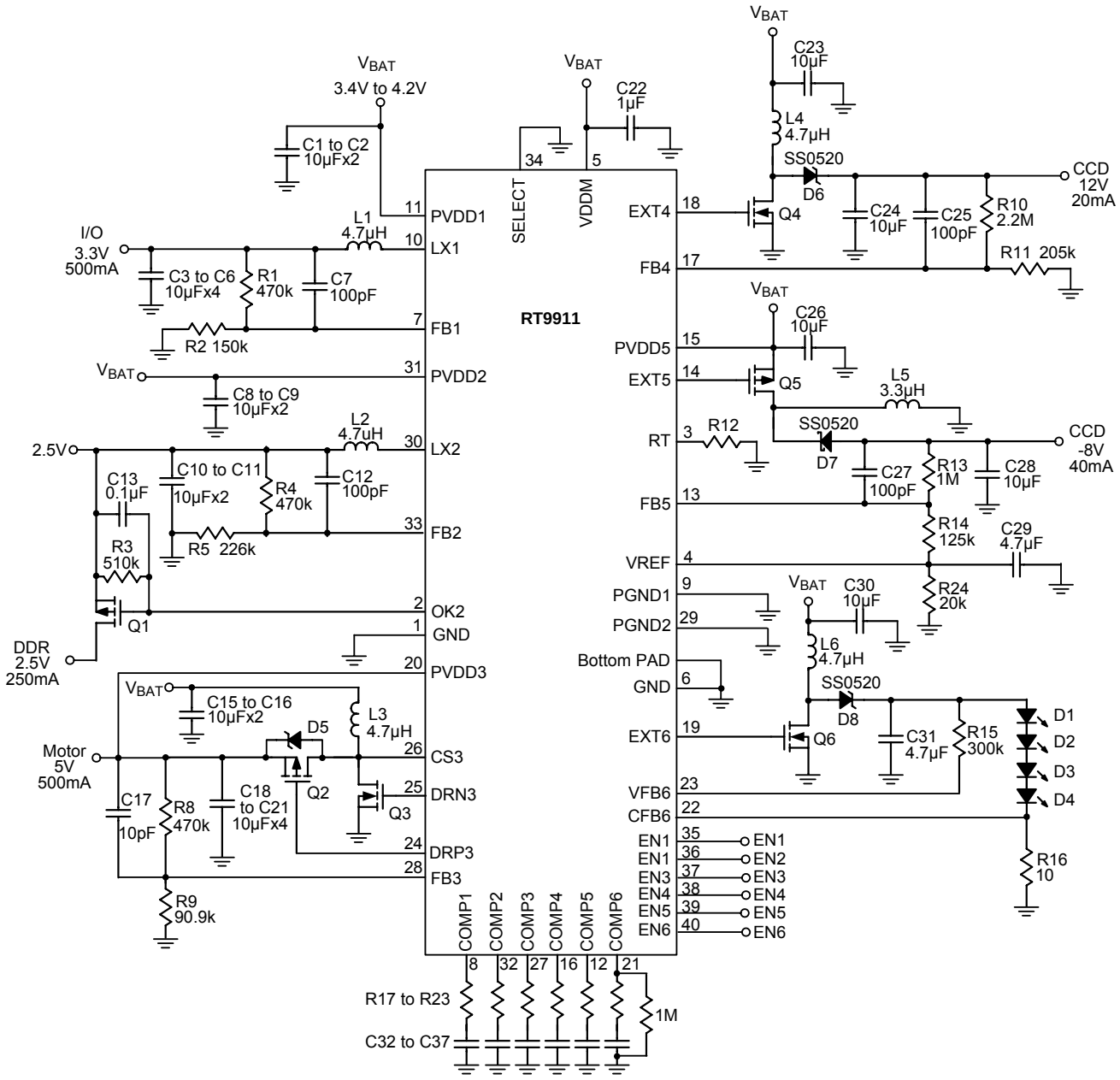



Figure 2. Application Circuit for Li-ion Battery Supply

Note :

- Bottom pad is GND pad, can be short to pin 6 (GND).
- Please remove Q2 when use Async Boost and remove D5 when use Sync Boost.
- Output voltage setting

  CH1: 0.8Vx(1+R1/R2) ex: I/O 3.3V = 0.8x(1+470k/150k)

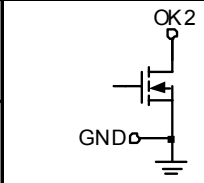
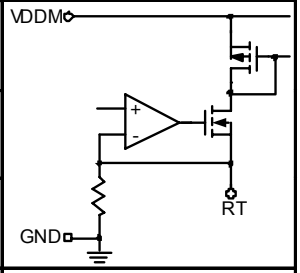
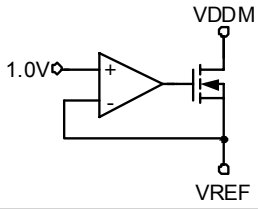
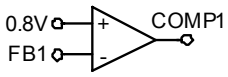
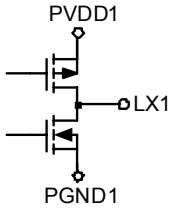
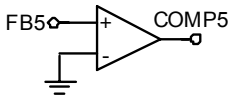
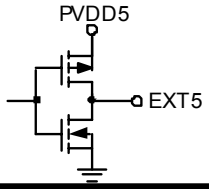
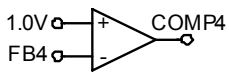
  CH2: 0.8Vx(1+R4/R5) ex: DDR 2.5V = 0.8x(1+470k/226k)

  CH3: 0.8Vx(1+R8/R9) ex: MOTOR 5V = 0.8x(1+470k/90.9k)

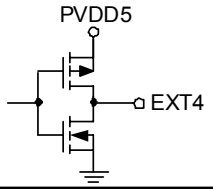
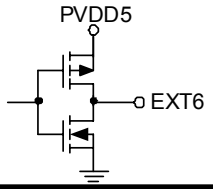
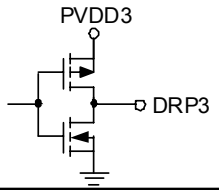
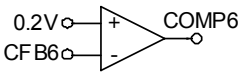
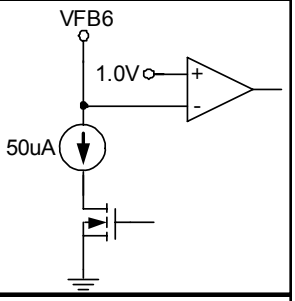
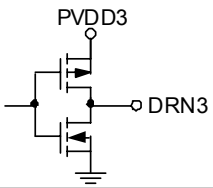
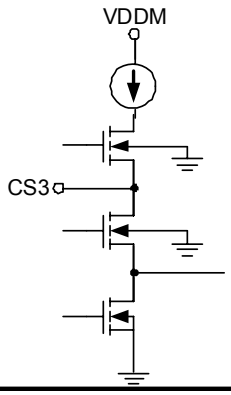
  CH4: 1.0Vx(1+R10/R11) ex: CCD 12V = 1.0x(1+2.2M/205k)

  CH5: -1.0Vx(R13/R14) ex: CCD -8V = -1.0x(1M/125k)

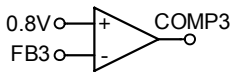
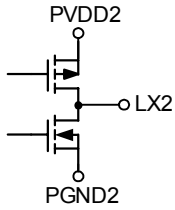
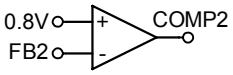
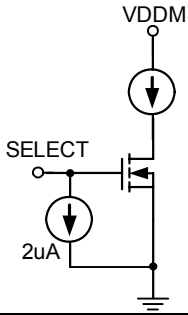
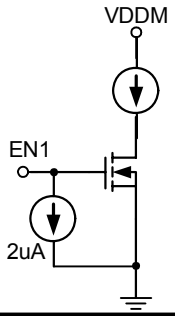
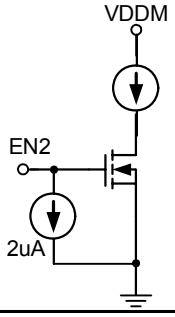
## Functional Pin Description

| Pin No. | Pin Name | Pin Function | I/O | Internal State at Shut Down | I/O Configuration |
|---|---|---|---|---|---|
| 1 | GND | Analog Ground Pin | -- | – |   |
| 2 | OK2 | External Switch Control. | OUT | High Impedance | |
| 3 | RT | Frequency Setting Pin. Frequency is 500kHz if RT pin not connected. | OUT | Pull Low |   |
| 5 | VDDM | Device Input Power Pin | IN | – | |
| 6 | GND | Analog Ground Pin | -- | – | |
| 4 | VREF | 1.0V Reference Pin | OUT | High Impedance |   |
| 7 | FB1 | Feedback Input Pin of CH1. | IN | High Impedance |   |
| 8 | COMP1 | Feedback Compensation Pin of CH1. | OUT | Pull Low | |
| 9 | PGND1 | Power Ground Pin of CH1. | -- | – |   |
| 10 | LX1 | Switch Node of CH1. | OUT | High Impedance | |
| 11 | PVDD1 | Power Input Pin of CH1. | IN | – | |
| 12 | COMP5 | Feedback Compensation Pin of CH5. | OUT | Pull Low |   |
| 13 | FB5 | Feedback Input Pin of CH5. | IN | High Impedance | |
| 14 | EXT5 | External Power Switch of CH5. | OUT | Pull High |   |
| 15 | PVDD5 | Power Input Pin of CH4, CH5 and CH6. | IN | – | |
| 16 | COMP4 | Feedback Compensation Pin of CH4. | OUT | Pull Low |   |
| 17 | FB4 | Feedback Input Pin of CH4. | IN | High Impedance | |

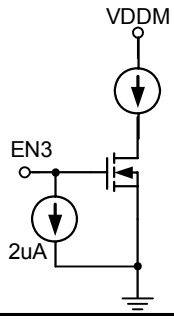
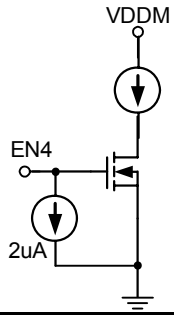
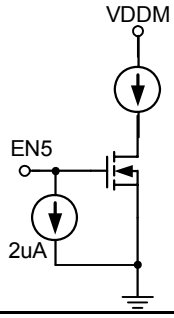
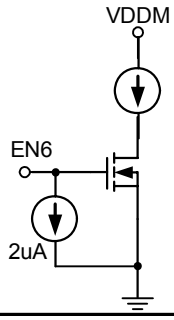
*To be continued*

| Pin No. | Pin Name | Pin Function | I/O | Internal State at Shut Down | I/O Configuration |
|---|---|---|---|---|---|
| 18 | EXT4 | External Power Switch of CH4. | OUT | Pull Low |  |
| 19 | EXT6 | External Power Switch of CH6. | OUT | Pull Low |  |
| 20 | PVDD3 | Power Input Pin of CH3. | IN | -- |  |
| 24 | DRP3 | External PMOS Switch Pin for CH3. | OUT | Pull High | |
| 21 | COMP6 | Feedback Compensation Pin of CH6. | OUT | Pull Low |  |
| 22 | CFB6 | Current Feedback Input Pin for CH6. | IN | High Impedance | |
| 23 | VFB6 | Voltage Feedback Input Pin for CH6. | IN | High Impedance |  |
| 25 | DRN3 | External NMOS Switch Pin for CH3. | OUT | Pull Low |  |
| 26 | CS3 | Current Sense Input Pin for CH3 | IN | High Impedance |  |

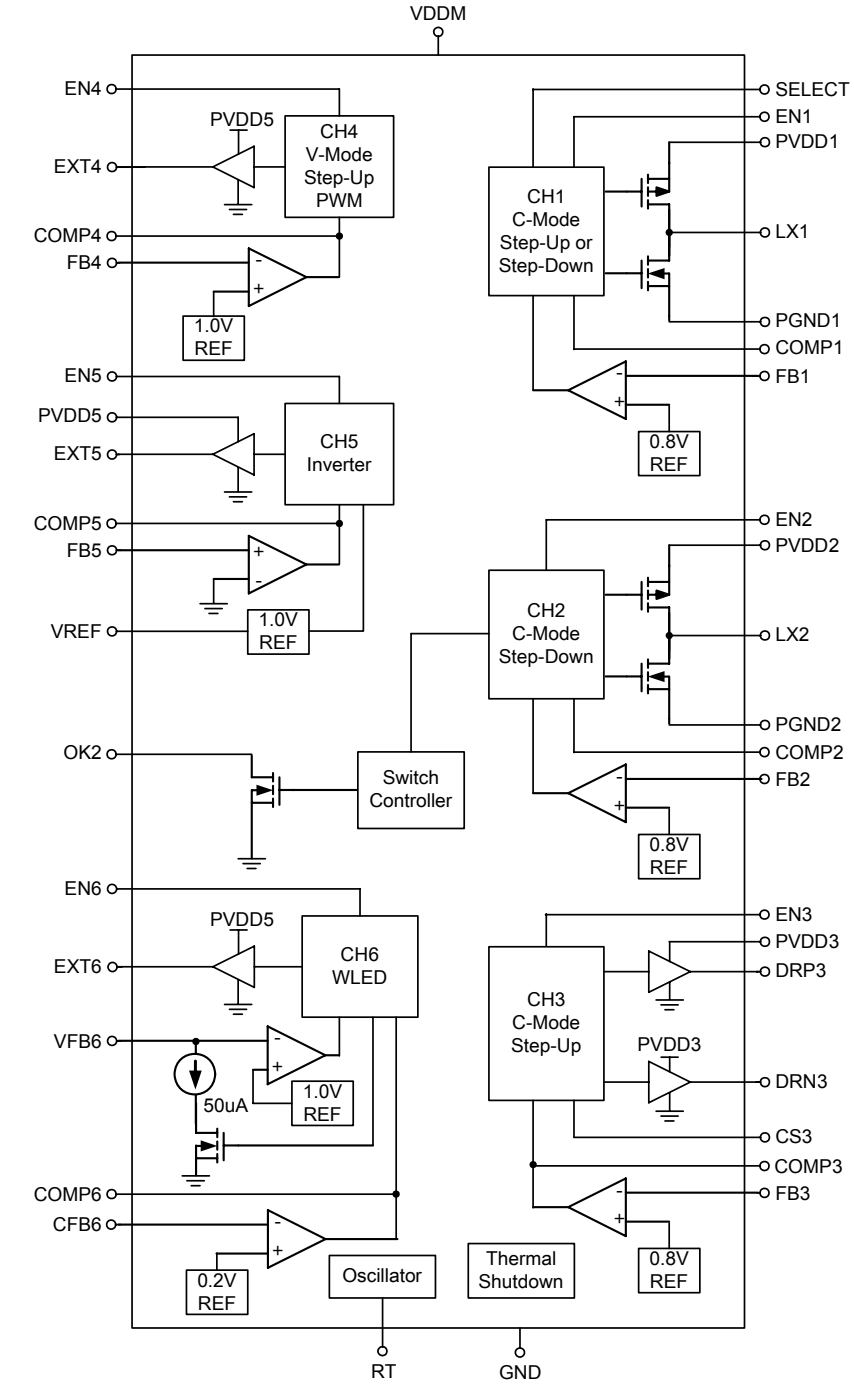
*To be continued*

| Pin No. | Pin Name | Pin Function | I/O | Internal State at Shut Down | I/O Configuration |
|---|---|---|---|---|---|
| 27 | COMP3 | Feedback Compensation Pin of CH3 | OUT | Pull Low |  |
| 28 | FB3 | Feedback Input Pin of CH3. | IN | High Impedance | |
| 29 | PGND2 | Power Ground Pin of CH2 | -- | -- |  |
| 30 | LX2 | Switch Node of CH2 | OUT | High Impedance | |
| 31 | PVDD2 | Power Input Pin of CH2. | IN | -- | |
| 32 | COMP2 | Feedback Compensation Pin of CH2. | OUT | Pull Low |  |
| 33 | FB2 | Feedback Input Pin of CH2. | IN | High Impedance | |
| 34 | SELECT | CH1 Boost/Buck Selection Pin. Logic state can't be changed during operation. | IN | Pull Low |  |
| 35 | EN1 | Enable Input Pin of CH1. | IN | Pull Low |  |
| 36 | EN2 | Enable Input Pin of CH2. | IN | Pull Low |  |

*To be continued*

| Pin No. | Pin Name | Pin Function | I/O | Internal State at Shut Down | I/O Configuration |
|---|---|---|---|---|---|
| 37 | EN3 | Enable Input Pin of CH3. | IN | Pull Low |  |
| 38 | EN4 | Enable Input Pin of CH4. | IN | Pull Low |  |
| 39 | EN5 | Enable Input Pin of CH5. | IN | Pull Low |  |
| 40 | EN6 | Enable Input Pin of CH6. | IN | Pull Low |  |
| Exposed Pad (41) | GND | The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation. | -- | -- | -- |

## Function Block Diagram



## Absolute Maximum Ratings (Note 1)

- Supply Voltage, $V_{DDM}$ ---------- –0.3V to 7V
- Power Switch ---------- –0.3V to ($V_{DD}$ + 0.3V)
- The Other Pins ---------- –0.3V to 7V
- Power Dissipation, $P_D$ @ $T_A$ = 25°C
  VQFN–40L 6x6 ---------- 2.778W
- Package Thermal Resistance (Note 2)
  VQFN-40L 6x6, $\theta_{JA}$ ---------- 36°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

## Recommended Operating Conditions (Note 4)

- Dimming Control Frequency Range, CH6 ---------- 300Hz to 900Hz
- Supply Voltage, $V_{DDM}$ ---------- 2.4V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Operation Temperature Range ---------- –40°C to 85°C

## Electrical Characteristics

($V_{DDM}$ = 3.3V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| VDDM Minimum Startup Voltage | $V_{ST}$ | (Note 5) | -- | -- | 1.6 | V |
| VDDM Operating Voltage | $V_{DDM}$ | VDDM Pin Voltage | 2.4 | -- | 5.5 | V |
| VDDM Over Voltage Protection | | | 5.9 | 6.5 | -- | V |
| **Supply Current** | | | | | | |
| Shutdown Supply Current into VDDM | $I_{OFF}$ | EN1 = EN2 = EN3 = EN4 = EN5 = EN6 = 0V | -- | 1 | 10 | μA |
| CH1 (Sync-Boost or Syn-Buck) Supply Current into VDDM | $I_{Q1}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 430 | μA |
| CH2 (Sync-Buck) Supply Current into VDDM | $I_{Q2}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 350 | μA |
| CH3 (Sync-Boost) Supply Current into VDDM | $I_{Q3}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 350 | μA |
| CH4 (Asyn-Boost) Supply Current into VDDM | $I_{Q4}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 300 | μA |
| CH5 (Asyn-Inverter) Supply Current into VDDM | $I_{Q5}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 300 | μA |
| CH6 (Asyn-Boost) Supply Current into VDDM | $I_{Q6}$ | $V_{DDM}$ = 3.3V, Non-Switching | -- | -- | 350 | μA |

*To be continued*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Oscillator** | | | | | | |
| Operation Frequency | $f_{OSC}$ | RT Open | 450 | 550 | 650 | kHz |
| CH1 Maximum Duty Cycle (Boost) | $D_{MAX1}$ | SELECT = 3.3V, $V_{FB1}$ = 0.7V | 80 | 85 | 90 | % |
| CH1 Maximum Duty Cycle (Buck) | $D_{MAX1}$ | SELECT = 0V, $V_{FB1}$ = 0.7V | 100 | -- | -- | % |
| CH2 Maximum Duty Cycle | $D_{MAX2}$ | $V_{FB2}$ = 0.7V | 100 | -- | -- | % |
| CH3 Maximum Duty Cycle | $D_{MAX3}$ | $V_{FB3}$ = 0.7V | 75 | 80 | 90 | % |
| CH4 Maximum Duty Cycle | $D_{MAX4}$ | $V_{FB4}$ = 0.9V | 90 | 94 | 98 | % |
| CH5 Maximum Duty Cycle | $D_{MAX5}$ | $V_{FB5}$ = 0.1V | | | | |
| CH6 Maximum Duty Cycle | $D_{MAX6}$ | $V_{CFB6}$ = 0.18V, $V_{FB6}$ = 0.9V | | | | |
| **Feedback Regulation Voltage** | | | | | | |
| Feedback Regulation Voltage @ FB1, FB2, FB3 | $V_{FB1, 2,3}$ | | 0.788 | 0.8 | 0.812 | V |
| Feedback Regulation Voltage @FB4 | $V_{FB4}$ | | 0.98 | 1 | 1.02 | V |
| Feedback Regulation Voltage @ FB5 | $V_{FB5}$ | | −15 | -- | +15 | mV |
| Feedback Regulation Voltage @ VFB6 | $V_{VFB6}$ | | -- | 1 | -- | V |
| Feedback Regulation Voltage @ CFB6 | $V_{CFB6}$ | | 0.18 | 0.2 | 0.22 | V |
| **Reference** | | | | | | |
| VREF Output Voltage | $V_{REF}$ | | 0.984 | 1 | 1.016 | V |
| VREF Load Regulation | | 0μA < $I_{REF}$ < 100μA | -- | -- | 10 | mV |
| **Error Amplifier** | | | | | | |
| GM (CH1, CH2, CH3, CH4, CH5, CH6) | | | -- | 0.2 | -- | ms |
| Compensation Source Current (CH1, CH2, CH3, CH4, CH5, CH6) | | | -- | 22 | -- | μA |
| Compensation Sink Current (CH1, CH2, CH3, CH4, CH5, CH6) | | | -- | 22 | -- | μA |
| **Power Switch** | | | | | | |
| CH1 On Resistance of MOSFET | $R_{DS(ON)P1}$ | P-MOSFET, $PV_{DD1}$ = 3.3V | -- | 200 | 300 | mΩ |
| | $R_{DS(ON)N1}$ | N-MOSFET, $PV_{DD1}$ = 3.3V | -- | 200 | 300 | mΩ |
| CH1 Switch Current Limitation (Buck) | | SELECT=0 | 1.3 | 2 | 4 | A |
| CH1 Switch Current Limitation (Boost) | | SELECT=1 | 2 | 2.5 | 4 | A |
| CH2 On Resistance of MOSFET | $R_{DS(ON)P2}$ | P-MOSFET, $PV_{DD2}$ = 3.3V | -- | 300 | 450 | mΩ |
| | $R_{DS(ON)N2}$ | N-MOSFET, $PV_{DD2}$ = 3.3V | -- | 300 | 450 | mΩ |
| CH2 Switch Current Limitation | | | 1.3 | 2 | 4 | A |
| CH3 On Resistance of DRN3 | $R_{DS(ON)NP3}$ | P-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |
| | $R_{DS(ON)NN3}$ | N-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |
| CH3 On Resistance of DRP3 | $R_{DS(ON)PP3}$ | P-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |
| | $R_{DS(ON)PN3}$ | N-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |
| CH4 On Resistance of MOSFET | $R_{DS(ON)P4}$ | P-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |
| | $R_{DS(ON)N4}$ | N-MOSFET, $PV_{DD3}$ = 3.3V | -- | 6 | 15 | Ω |

*To be continued*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Power Switch** | | | | | | |
| CH5 On Resistance of MOSFET | $R_{DS(ON)P5}$ | P-MOSFET, $PV_{DD5}$ = 3.3V | -- | 6 | 15 | Ω |
| | $R_{DS(ON)N5}$ | N-MOSFET, $PV_{DD5}$ = 3.3V | -- | 6 | 15 | Ω |
| CH6 On Resistance of MOSFET | $R_{DS(ON)P6}$ | P-MOSFET, $PV_{DD5}$ = 3.3V | -- | 6 | 15 | Ω |
| | $R_{DS(ON)N6}$ | N-MOSFET, $PV_{DD5}$ = 3.3V | -- | 6 | 15 | Ω |
| **Switch Controller** | | | | | | |
| OK2 pin Sink Current | | OK2 = 1V | 90 | -- | -- | μA |
| **External Current Setting (CH3)** | | | | | | |
| CS3 Sourcing Current | $I_{CS3}$ | | 5 | 10 | 15 | μA |
| VFB6 Sink Current | $I_{VFB6}$ | | 40 | 50 | 60 | μA |
| **Protection** | | | | | | |
| Under Voltage Protection Threshold Voltage @ FB1, FB2 | | SELECT = 0V | 0.3 | 0.4 | 0.5 | V |
| Over Voltage Protection @ FB1, FB2 | | SELECT = 0V | -- | 1 | -- | V |
| **Control** | | | | | | |
| EN1, EN2, EN3, EN4, EN5, EN6 Input High Level Threshold | | $V_{DDM}$ = 3.3V | -- | -- | 1.3 | V |
| EN1, EN2, EN3, EN4, EN5, EN6 Input Low Level Threshold | | $V_{DDM}$ = 3.3V | 0.4 | -- | -- | V |
| EN1, EN2, EN3, EN4, EN5, EN6 Sink Current | | $V_{DDM}$ = 3.3V | -- | 2 | 6 | μA |
| Select Pin Input High Level Threshold | | | -- | -- | 1.3 | V |
| Select Pin Input Low Level Threshold | | | 0.4 | -- | -- | V |
| Select Pin Sink Current | $I_{SELECT}$ | | -- | 2 | 6 | μA |
| **Thermal Protection** | | | | | | |
| Thermal Shutdown | $T_{SD}$ | | 125 | 180 | -- | °C |
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | | -- | 20 | -- | °C |

**Note 1.** Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

**Note 2.** $\theta_{JA}$ is measured in the natural convection at $T_A$ = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

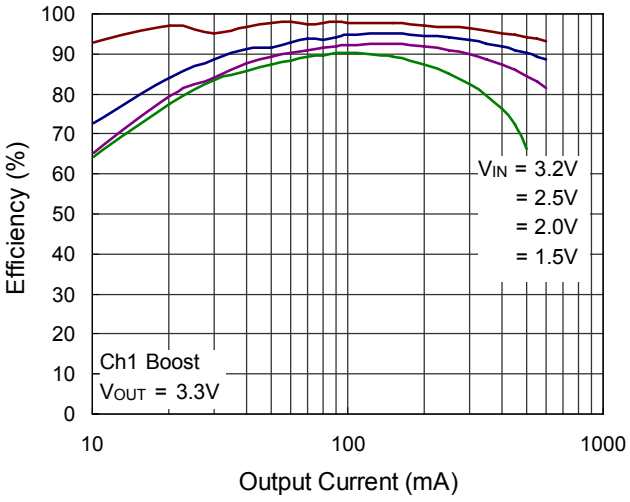
**Note 3.** Devices are ESD sensitive. Handling precaution recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

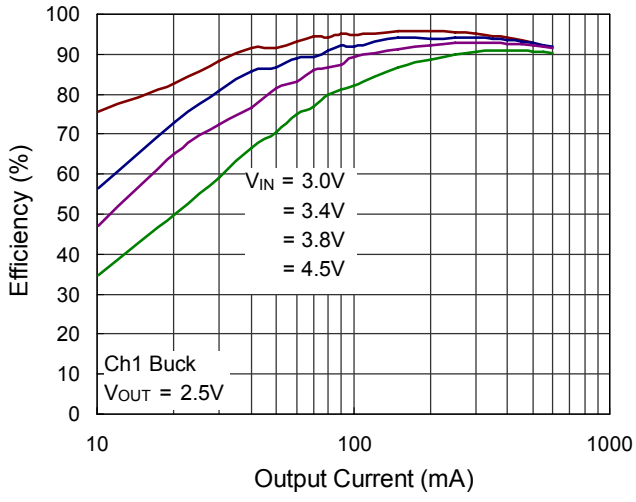
**Note 5.** A Schottky retifier connected from LX1 to PVDD1 is required for low-voltage startup, refer to Figure 1.

## Typical Operating Characteristics

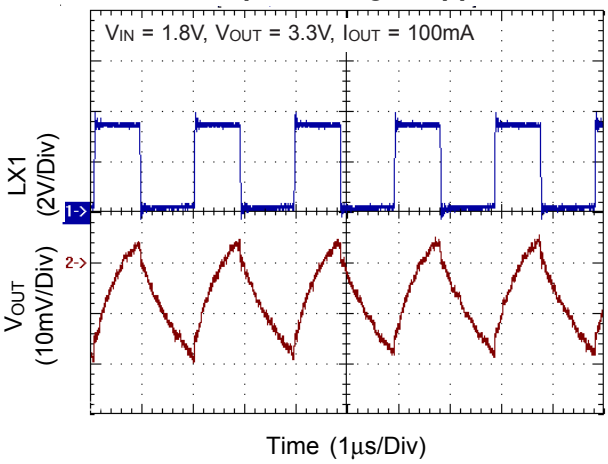
**CH1 Boost Efficiency vs. Output Current**



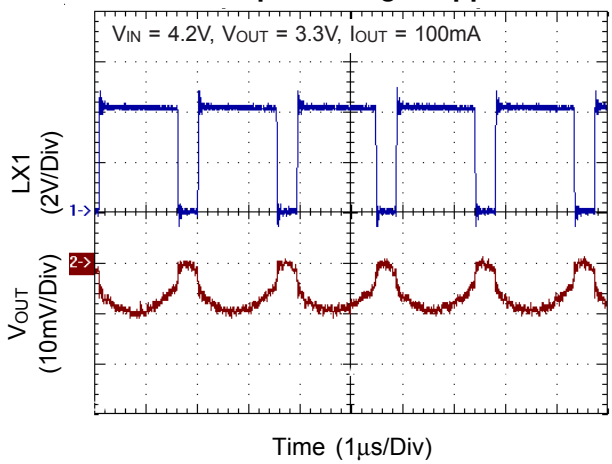

**CH1 Buck Efficiency vs. Output Current**



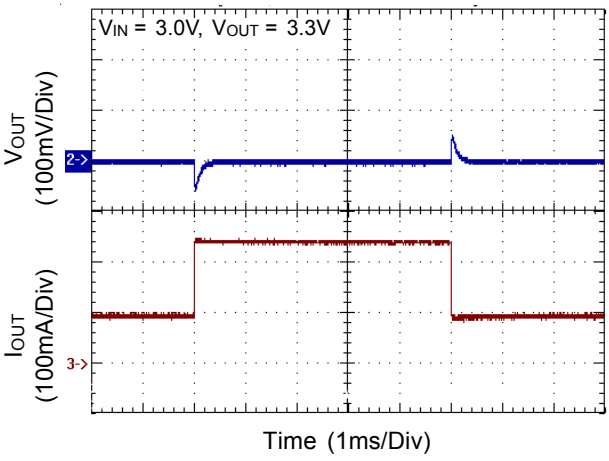

**CH1 Boost LX1 and Output Voltage Ripple**



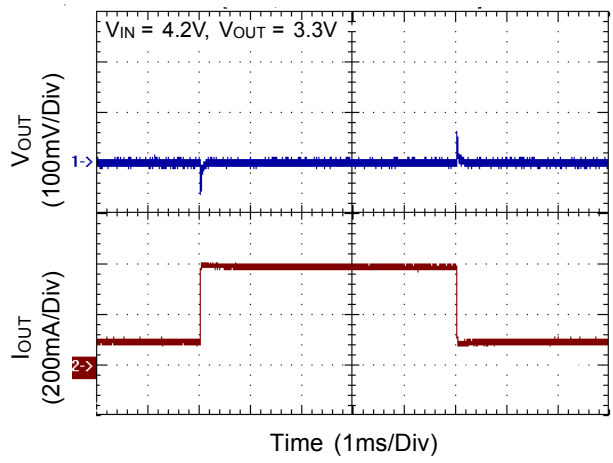

**CH1 Buck LX1 and Output Voltage Ripple**



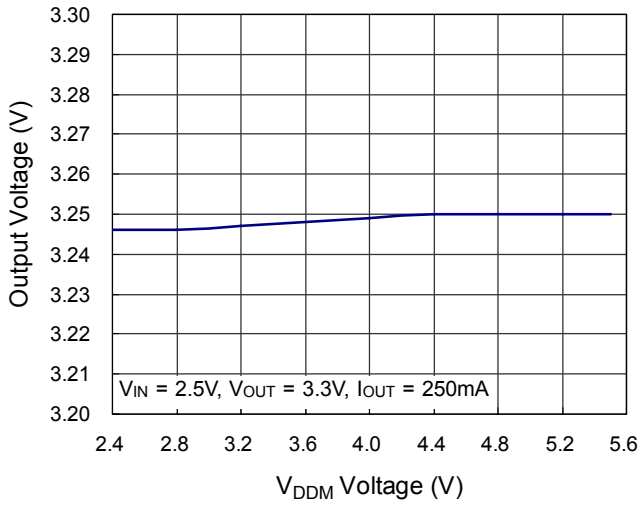

**CH1 Boost Load Transient Response**



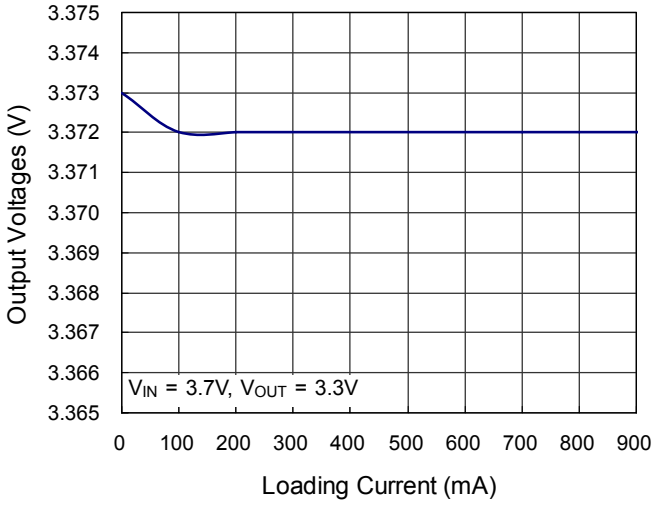

**CH1 Buck Load Transient Response**



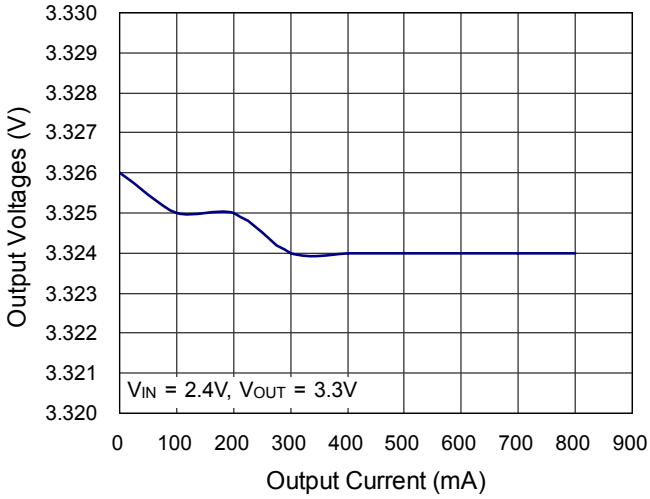
**CH1 Boost Output Voltage vs. $V_{DDM}$ Voltage**



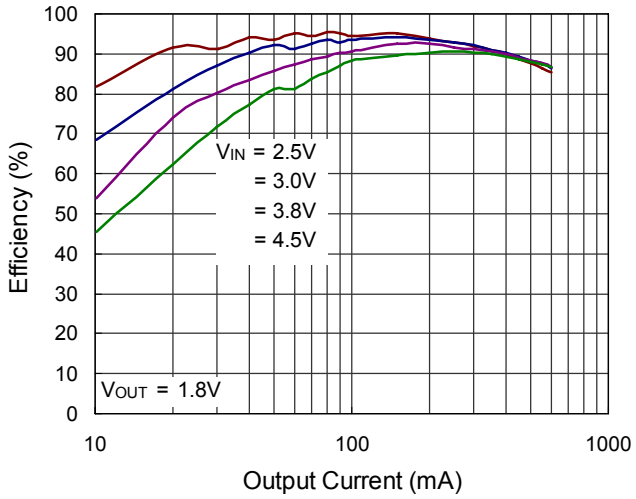

**CH1 Buck Output Voltage vs. Output Current**



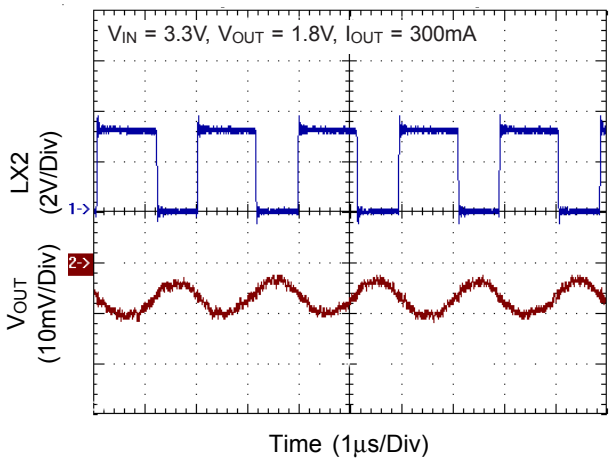

**CH1 Boost Output Voltage vs. Output Current**



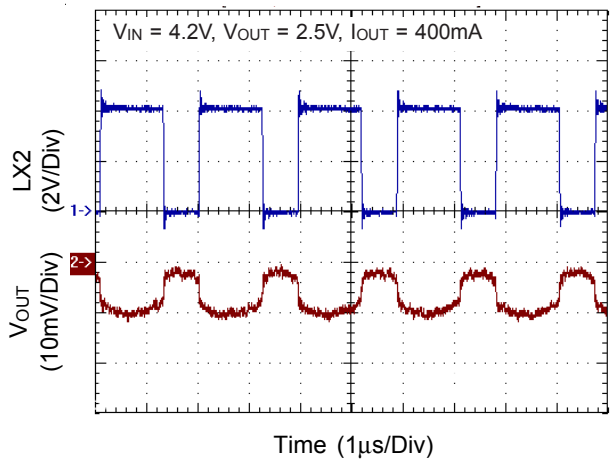

**CH2 Buck Efficiency vs. Output Current**



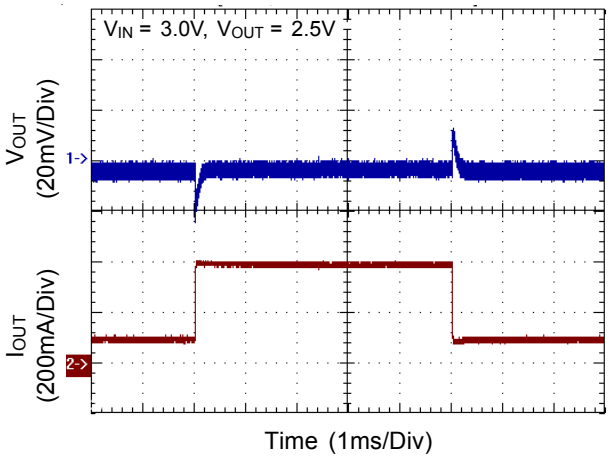

**CH2 LX2 and Output Voltage Ripple**



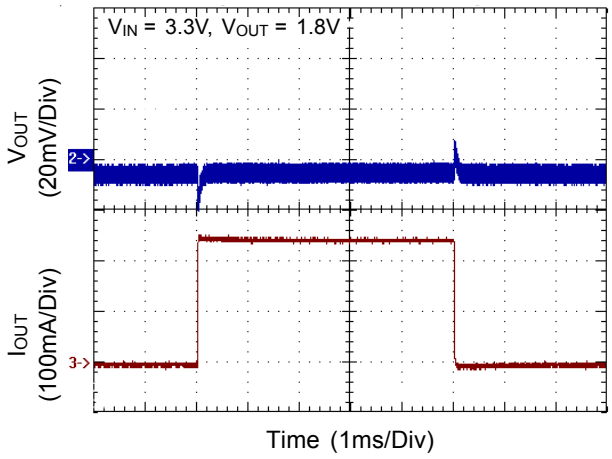

**CH2 LX2 and Output Voltage Ripple**



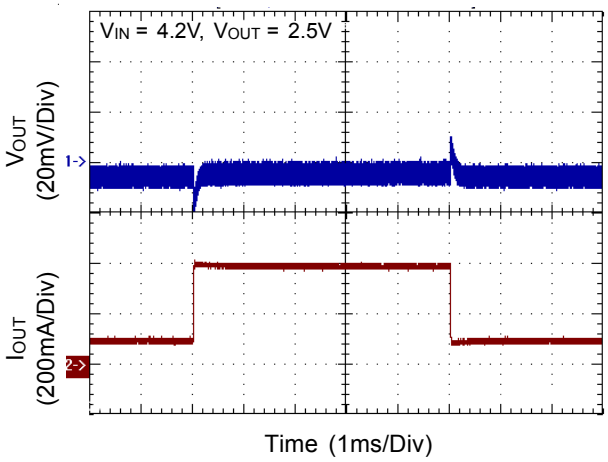
### CH2 Load Transient Response



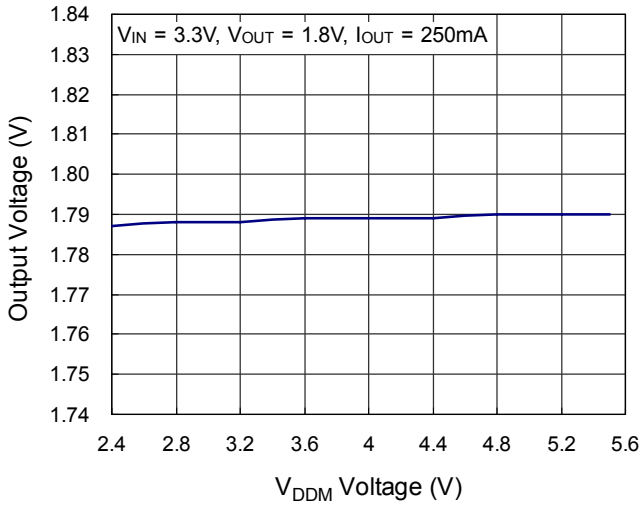

### CH2 Load Transient Response



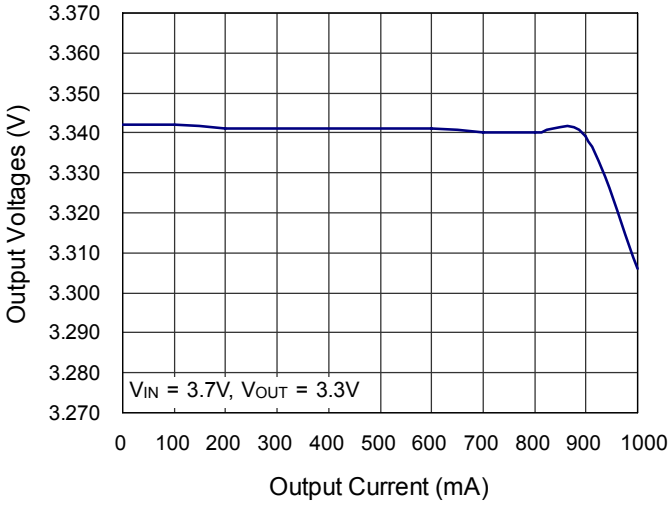

### CH2 Load Transient Response



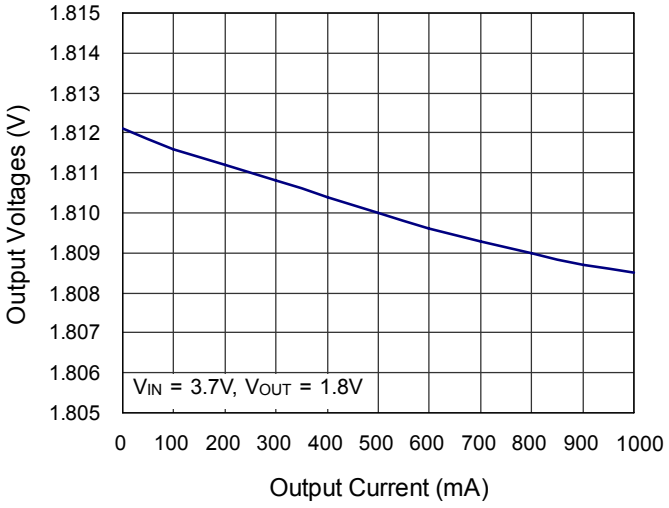

### CH2 Output Voltage vs. $V_{DDM}$ Voltage



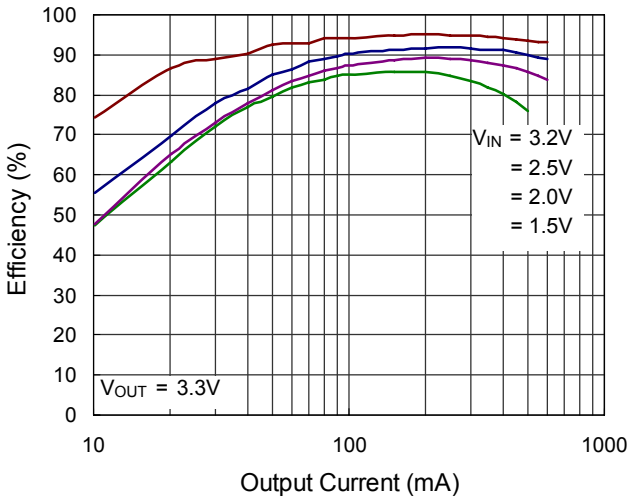

### CH2 Buck Output Voltage vs. Output Current



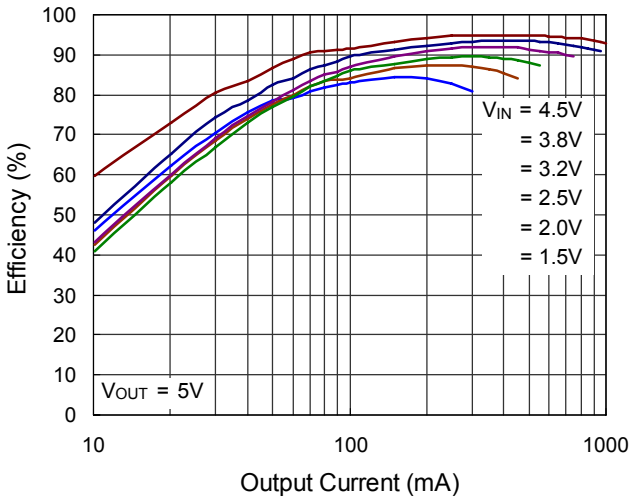

### CH2 Buck Output Voltage vs. Output Current



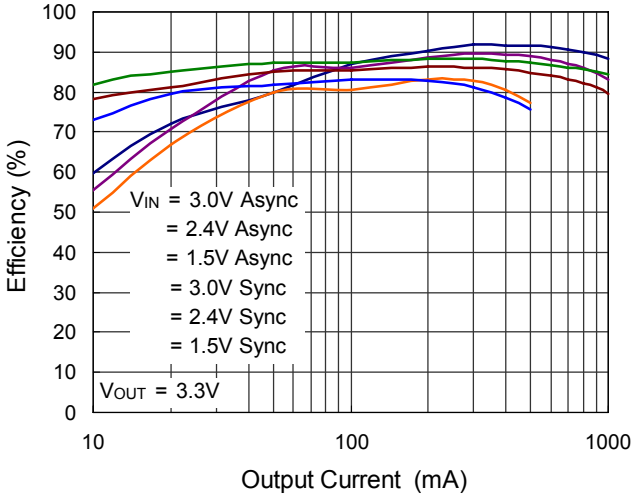
**CH3 Boost Efficiency vs. Output Current**



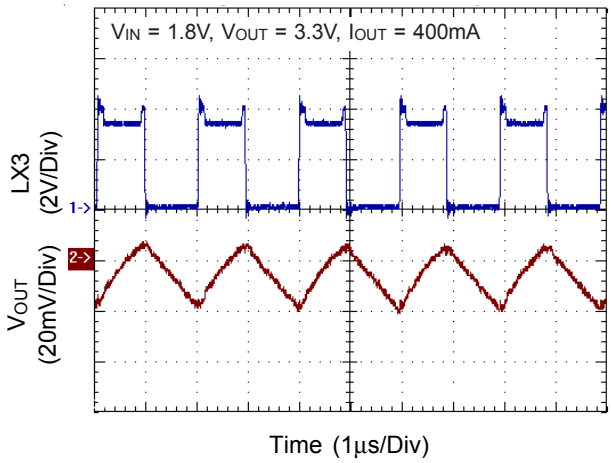

**CH3 Boost Efficiency vs. Output Current**



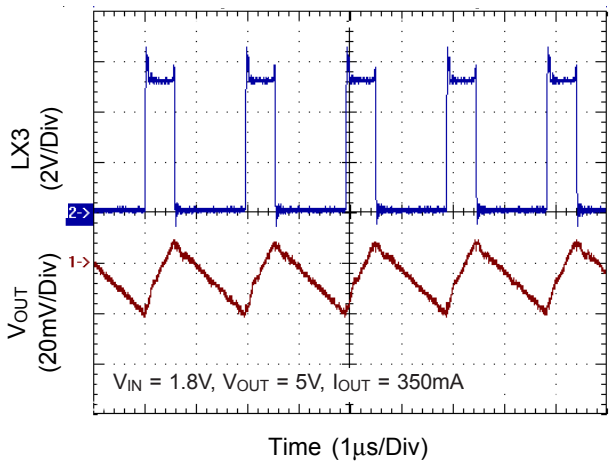

**CH3 Boost Efficiency vs. Output Current**



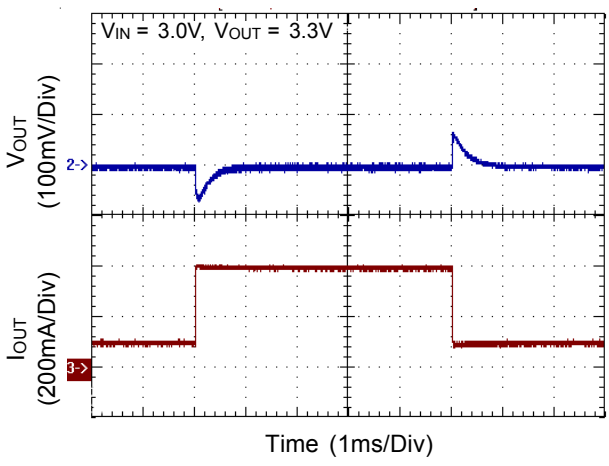

**CH3 LX3 and Output Voltage Ripple**



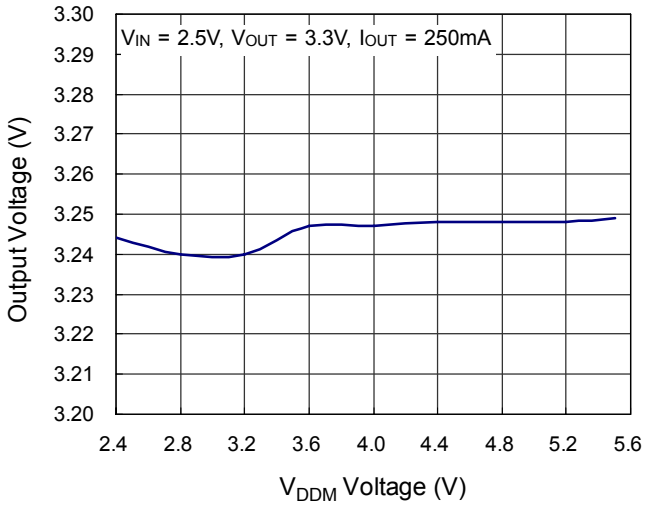

**CH3 LX3 and Output Voltage Ripple**



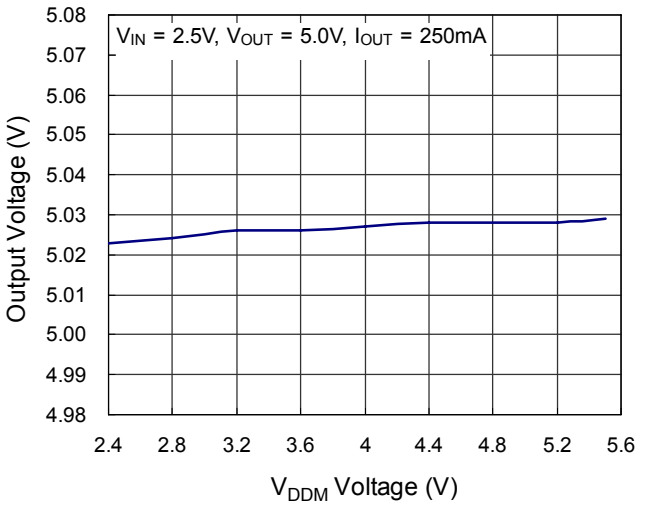

**CH3 Load Transient Response**



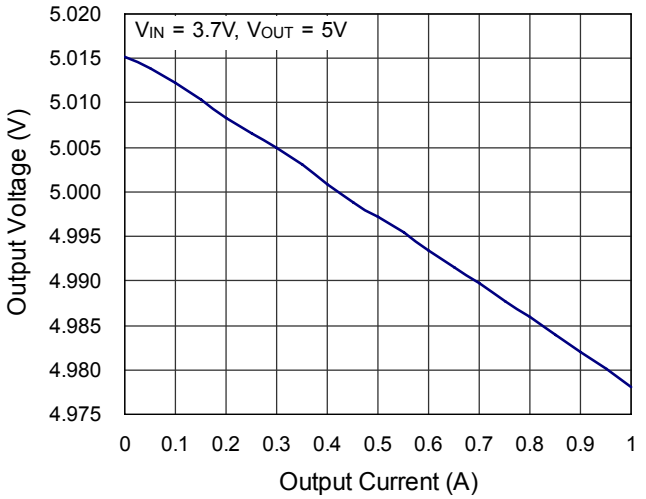
### CH3 Boost Output Voltage vs. $V_{DDM}$ Voltage



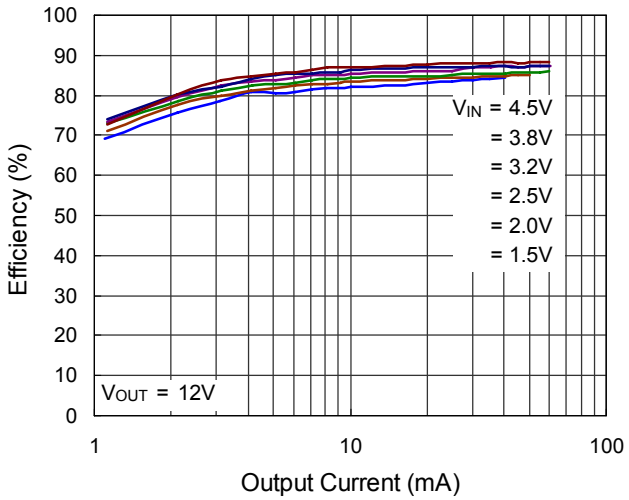

### CH3 Boost Output Voltage vs. $V_{DDM}$ Voltage



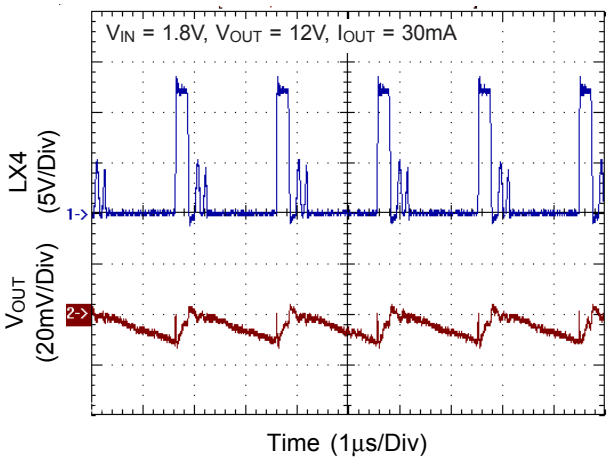

### CH3 Boost Output Voltage vs. Output Current



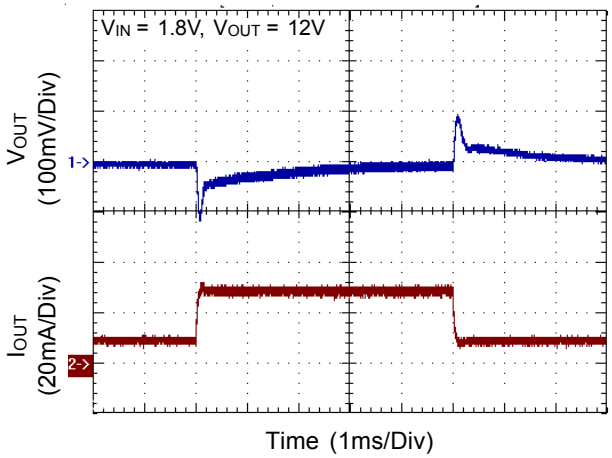

### CH4 Boost Efficiency vs. Output Current



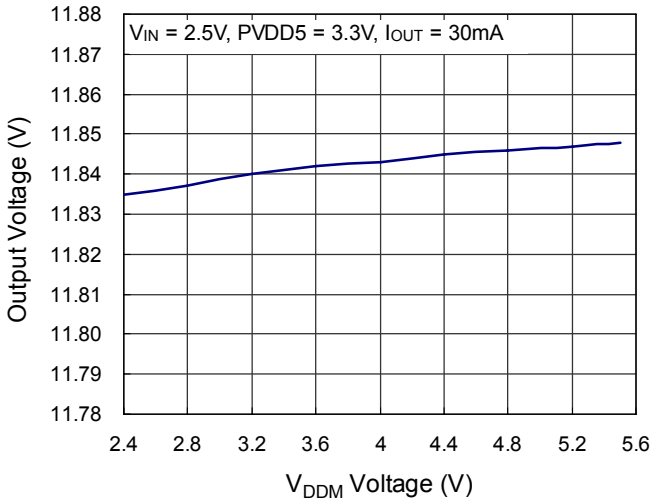

### CH4 LX4 and Output Voltage Ripple



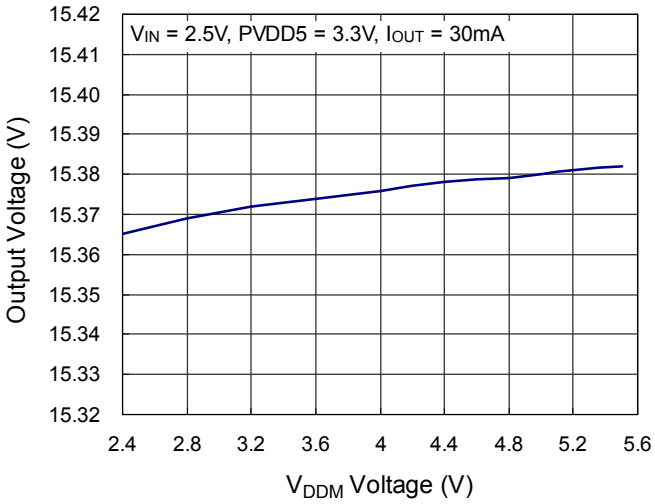

### CH4 Load Transient Response



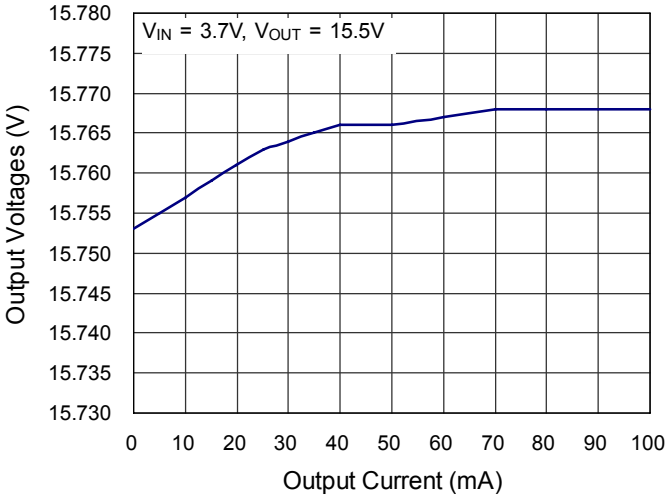
**CH4 Output Voltage vs. $V_{DDM}$ Voltage**



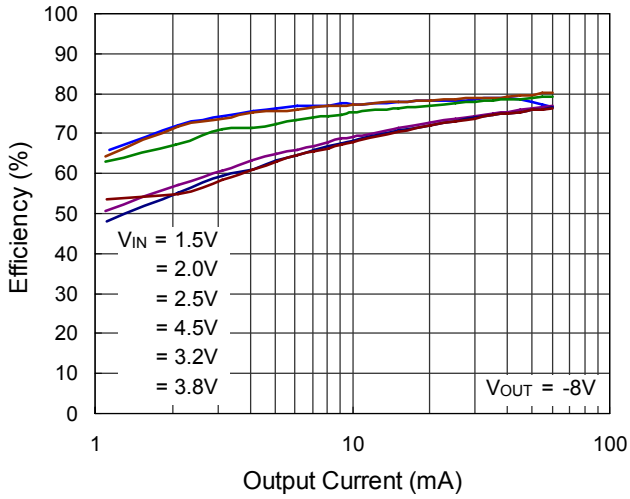

**CH4 Output Voltage vs. $V_{DDM}$ Voltage**



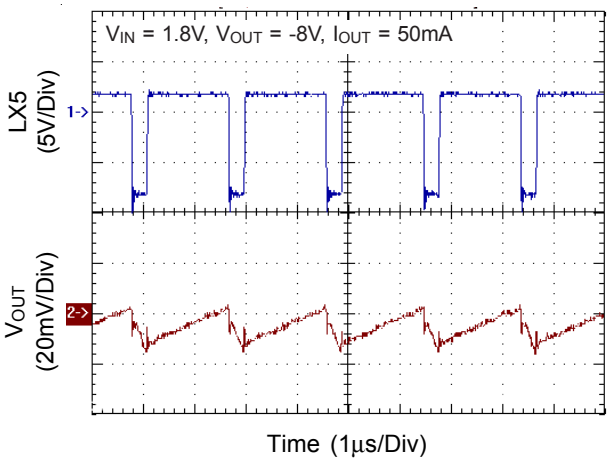

**CH4 Boost Output Voltage vs. Output Current**



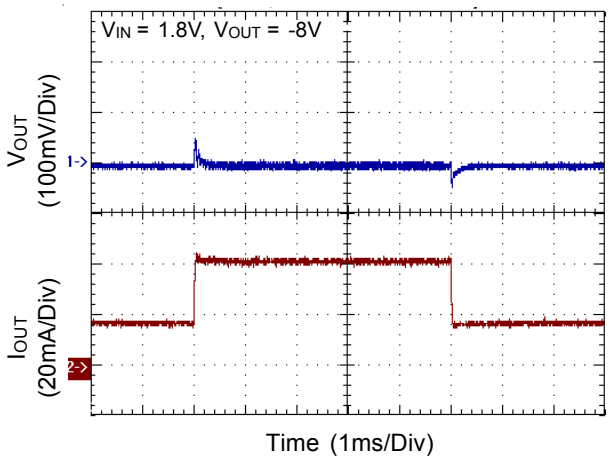

**CH5 Inverting Efficiency vs. Output Current**



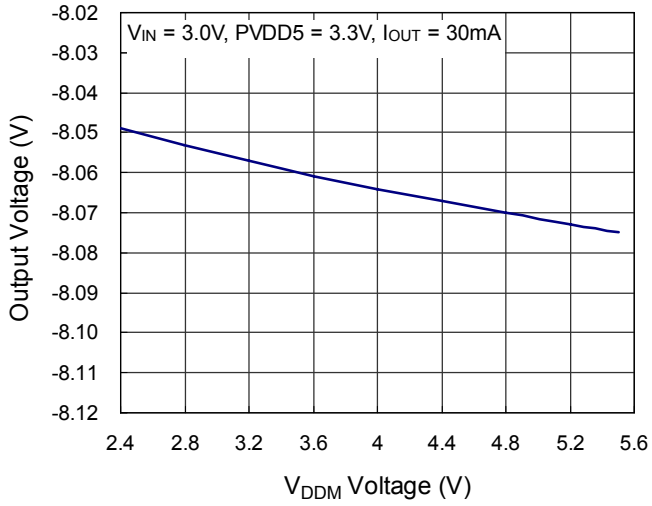

**CH5 LX5 and Output Voltage Ripple**



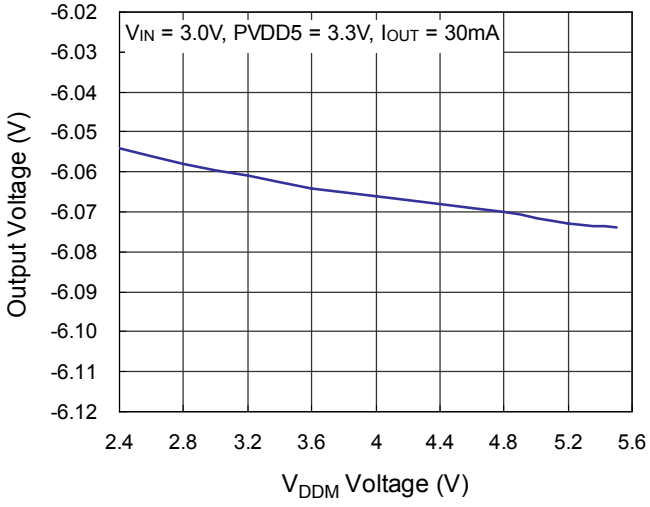

**CH5 Load Transient Response**



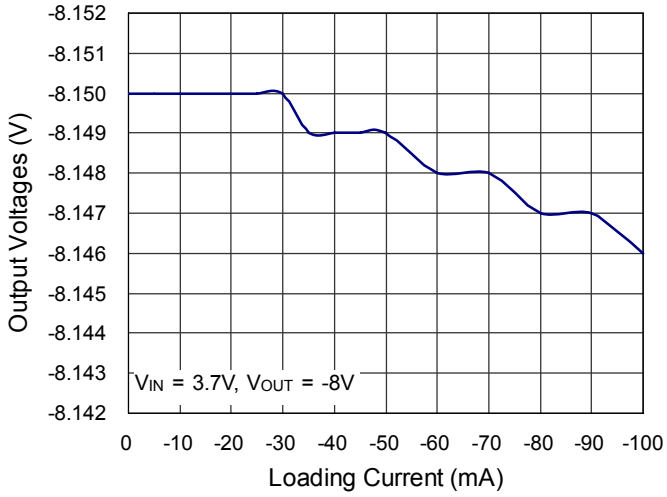
### CH5 Output Voltage vs. $V_{DDM}$ Voltage



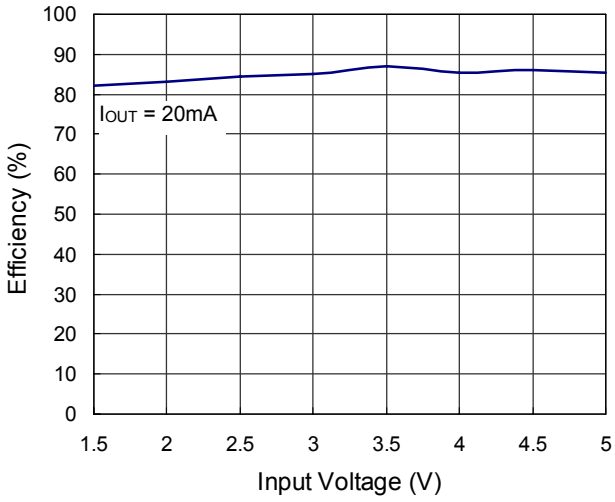

### CH5 Output Voltage vs. $V_{DDM}$ Voltage



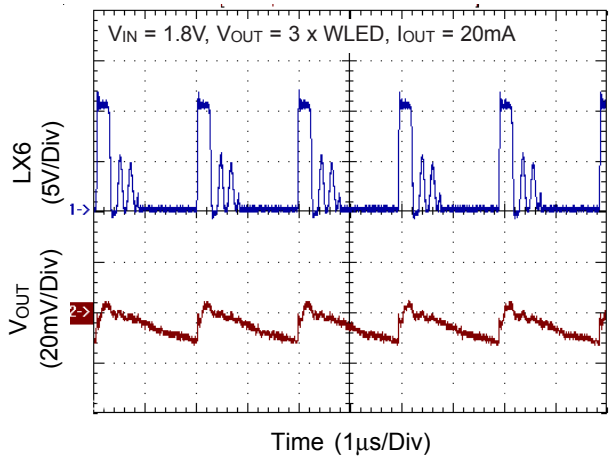

### CH5 Output Voltage vs. Output Current



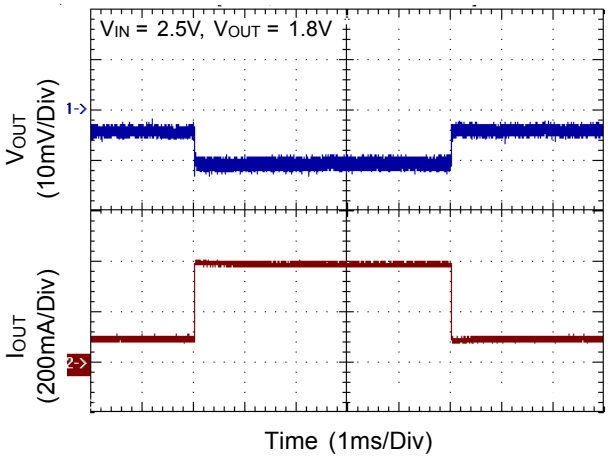

### CH6 Efficiency vs. Input Voltage



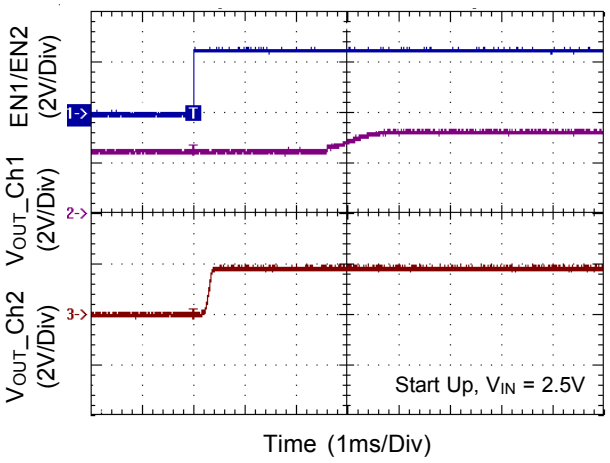

### CH6 LX6 and Output Voltage Ripple



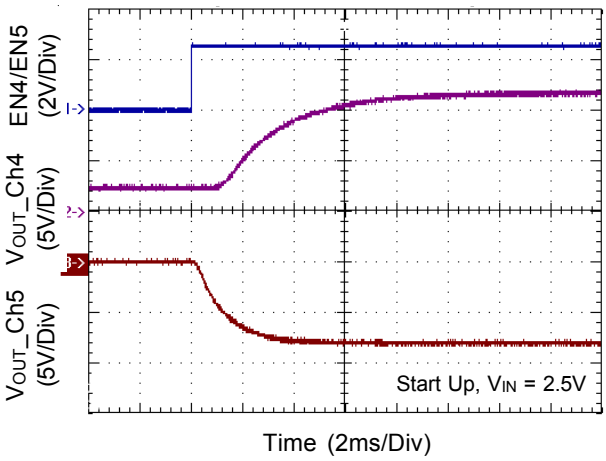

### CH7 Load Transient Response



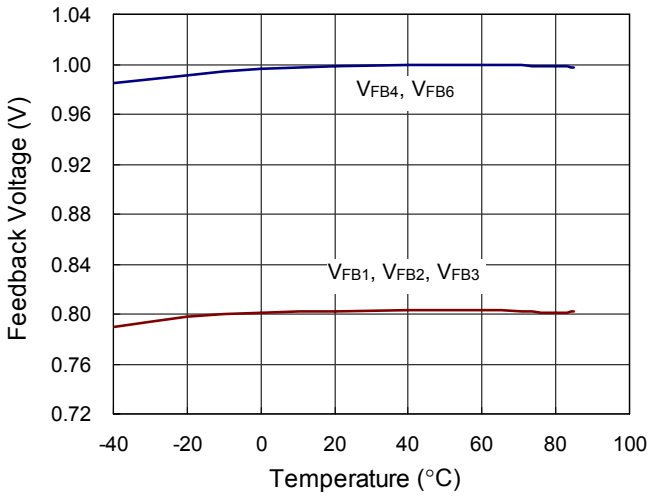
**CH1 and CH2 Power Sequence**




**CH4 and CH5 Power Sequence**




**Feedback Voltage vs. Temperature**



## Applications Information

The RT9911 includes the following six DC/DC converter channels to build a multiple-output power-supply system.

**CH1 :** Selectable step-up or step-down synchronous current mode DC/DC converter with internal power MOSFETs.

**CH2 :** Step-down synchronous current mode DC/DC converter with internal power MOSFETs.

**CH3 :** Step-up asynchronous current mode DC/DC controller to drive external power MOSFETs.

**CH4 :** Step-up asynchronous voltage mode DC/DC controller.

**CH5 :** Inverting DC/DC voltage mode controller.

**CH6 :** DC/DC voltage mode controller for WLED as well as conventional boost application; provides open LED OVP protection.

### CH1 : Selectable Step-up or Step-down Converter

CH1 is selectable as step-up (SELECT pin = logic high) or step-down (SELECT pin = logic low).

Step-up : With internal MOSFETs and synchronous rectifier, the efficiency is up to 95%. The converter always operates at fixed frequency PWM mode and CCM (continuous current mode).

Step-down : With internal MOSFETs and synchronous rectifier, the efficiency is up to 95%. The converter always operates at fixed frequency PWM mode and CCM. While the input voltage is close to output voltage, the converter enters low dropout mode. Duty could be as long as 100% to extend battery life. See Figure 3(a) for detailed functional block.

### CH2 : Step-down DC/DC Converter

With internal MOSFETs and synchronous rectifier, the efficiency is up to 95%. The converter always operates at fixed frequency PWM mode and CCM. While the input voltage is close to output voltage, the converter enters low dropout mode. Duty could be as long as 100% to extend battery life. See Figure 3(b) for detailed functional block.

### CH3 : Step-up DC/DC Controller

With external MOSFETs and a synchronous rectifier, the efficiency is up to 97%. The converter always operates at fixed frequency PWM mode and CCM. The threshold of current limit is estimated by $R_{DS(ON)}$ of external NMOS. See **Protections** for detailed information and detailed functional block in Figure 3(c).

### CH4, CH6 : Step-up DC/DC Controller

CH4 and CH6 are fixed frequency voltage mode PWM controllers. EXT4 and EXT6 pins are designed to drive external NMOS switch. CH6 is optimized for WLED application. CFB6 is current-sensing feedback, and VFB6 provides over voltage protection (WLED open circuit). See **Protections** for detailed information and detailed functional block in Figure 3(d for CH4 and e for CH6).

### CH5 : Inverting Controller

CH5 is a voltage mode, fixed frequency PWM controller to generate negative output voltage. EXT5 is designed to drive external PMOS switch. To turn off PMOS completely, please note that PVDD5 should not be lower than the source voltage of PMOS. See Figure 3(f) for detailed functional block.

### Reference Voltage

RT9911 provides a precise 1V reference voltage with souring capability 100μA. Connect a 1μF ceramic capacitor from VREF pin to GND. Reference voltage is enabled by connecting EN5 to logic high.

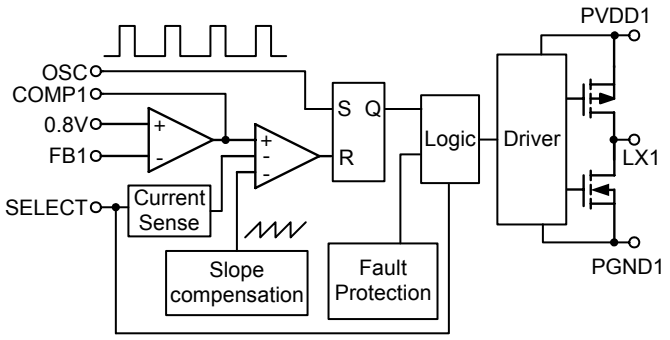



Figure 3(a)

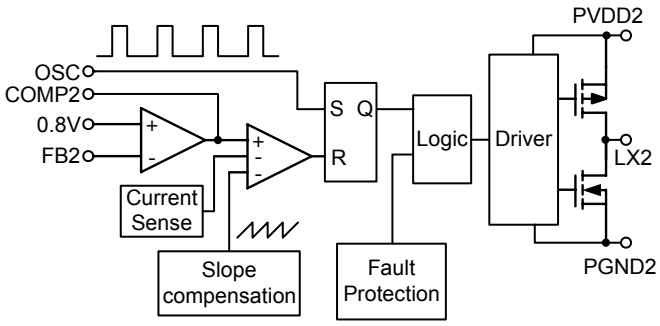



Figure 3(b)

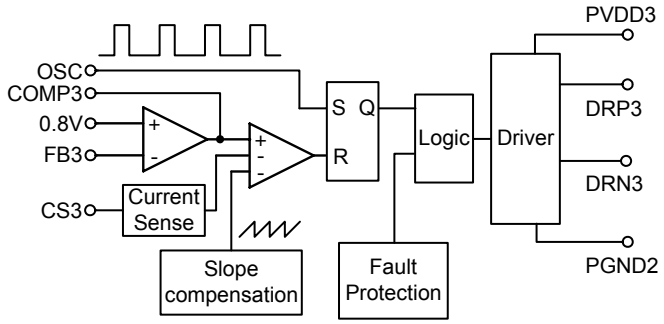



Figure 3(c)

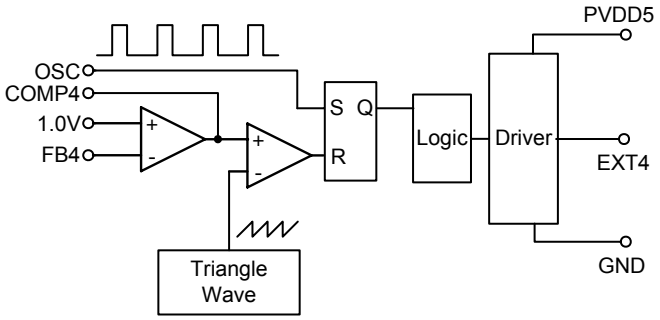



Figure 3(d)

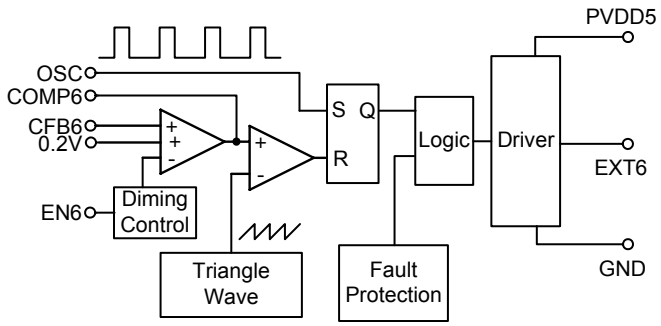



Figure 3(e)

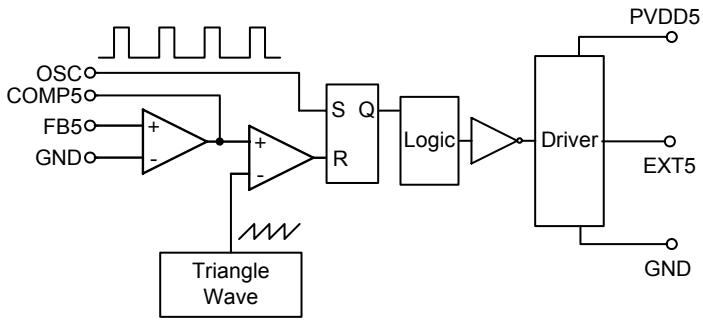
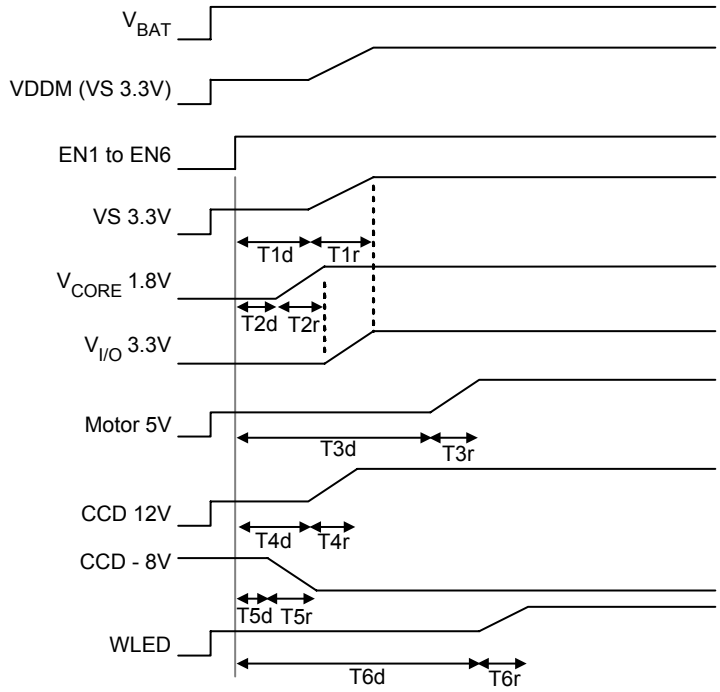



Figure 3(f)

Figure 3. Detailed Functional Block for each channel




Note :

- Please refer to Figure 1 for application Information.
- Timing sequence should be controlled by EN pins.

Figure 4. Timing Diagram

**Calculation method:**

Td1 to Td6 are precise value. Tr1 to Tr6 are approximation.

Units : T in second, C in Farad, R in Ohm

C31 to C36 : Compensation capacitor of CH1 to CH6.

T1d = 0.7V x C31 / 2μA (CH1 Boost)

T1d = 0.7V x C31 / 2μA (CH1 Buck)

T2d = 0.35V x C32 / 2μA

T3d = 0.7V x C33 / 2μA

T4d = 0.35V x C34 / 2μA

T5d = 0.85V x C35 / 2μA

T6d = 0.85V x C36 / 2μA

T1r = (0.5V x D1 + 0.48A x $R_{DS(ON)\_N}$ x C31 /1.25μA @ No load (Boost)

T1r = (0.33V x D1 + 0.2A x $R_{DS(ON)\_P}$ x C31 /1.25μA @ No load (Buck)

T2r = (0.33V x D2 + 0.2A x $R_{DS(ON)\_P}$ x C32 /1.25μA @ No load

T3r = (0.5V x D3 + 0.8A x $R_{DS(ON)\_N}$ x C33 /3.6μA @ No load

T4r = (1.0V x D4) x C34 / 1μA @ No load

T5r = (1.0V x D5) x C35 / 1μA @ 1mA min. load

T6r = (0.25V x D6) x C36 / 2.6μA @ 4 WLEDs

where

D1 = 1 – ($V_{BAT}$ / $V_{VS\ 3.3V}$) (Boost)

D1 = $V_{VS\ 3.3V}$ / $V_{BAT}$ (Buck)

D2 = $V_{VCORE\ 1.8V}$ / $V_{BAT}$

D3 = 1 – ($V_{BAT}$ / $V_{Motor\ 5V}$)

D4 = 1 – ($V_{BAT}$ / $V_{CCD\ 12V}$)

D5 = $|V_{CCD\ -8V}|$ / ( $V_{BAT}$ + $|V_{CCD\ -8V}|$)

D6 = 1 – ($V_{BAT}$ / $V_{WLED}$)

Example : T1d = 0.7V x 1nF / 2μA = 350μs (Boost)

T1r = (0.5 x (1–1.8/3.3) + 0.48 x 0.2) x 1nF / 1.25μA = 258μs

### Oscillator

The internal oscillator synchronizes CH1 to CH6 with fixed operation frequency. The frequency could be set by connecting resistor between RT pin to GND. See Figure 5 to adjust frequency.

### Soft Start

With internal soft start mechanism, the soft start time of each channel is proportional to the compensation capacitor. Refer to the soft start waveform in Figure 4 for typical application.

### Protection

RT9911 provides versatile protection functions. Protection type, threshold and protection methods are summarized in Table 1.

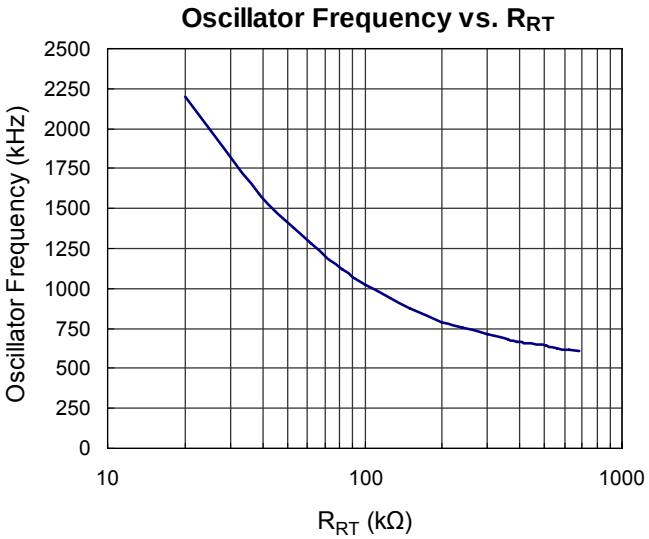



Figure 5. Adjust Frequency

**Table 1**

| | Protection type | Threshold (typical) Refer to Electrical spec | Protection methods | Reset method |
|---|---|---|---|---|
| VDDM | Over Voltage Protection | VDDM > 6.5V | Disable all channels | Restart if VDDM < 6.5V |
| CH1: Boost | Current Limit | NMOS current> 2.5A | NMOS latched off | Automatic reset at next clock cycle |
| CH1: Buck | Current Limit | PMOS current > 2.0A | PMOS latched off and all channels shutdown | VDDM power reset |
| | Under Voltage Protection | FB1 < 0.4V | NMOS, PMOS latch off and all channels shutdown | VDDM power reset |
| | Over Voltage Protection | FB1 > 1.0V | NMOS, PMOS latch off and all channels shutdown | VDDM power reset |
| CH2 | Current Limit | PMOS current > 2.0A | PMOS latched off and all channels shutdown | VDDM power reset |
| | Under Voltage Protection | FB2 < 0.4V | NMOS, PMOS latch off and all channels shutdown | VDDM power reset |
| | Over Voltage Protection | FB2 > 1.0V | NMOS, PMOS latch off and all channels shutdown | VDDM power reset |
| CH3 | Current Limit | CS3 > 0.3V, see below Note | NMOS latched off | Automatic reset at next clock cycle |
| CH6 | Over Voltage Protection | VFB6 > 1.0V, see Figure 8 | NMOS off | VFB6 < 1.0V |
| Thermal | Thermal shutdown | Temperature > 180°C | All channels stop switching | Temperature < 160°C |

**Note :** If $R_{DS(ON)}$ x $I_{inductor}$ > 0.3V, then current limit happens.

For example, if select NMOS( AOS3402), $R_{DS(ON)}$ =110mΩ (at $V_{GS}$ = 2.5V), then current limt happens if $I_{inductor}$ > 2.73A.

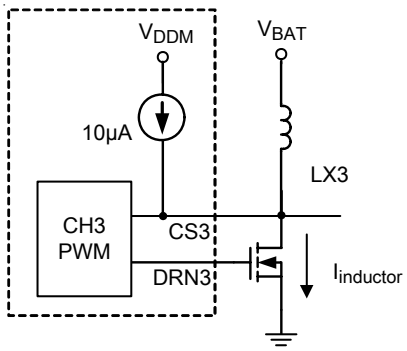



Figure 6. CH3 Current Limit Setting

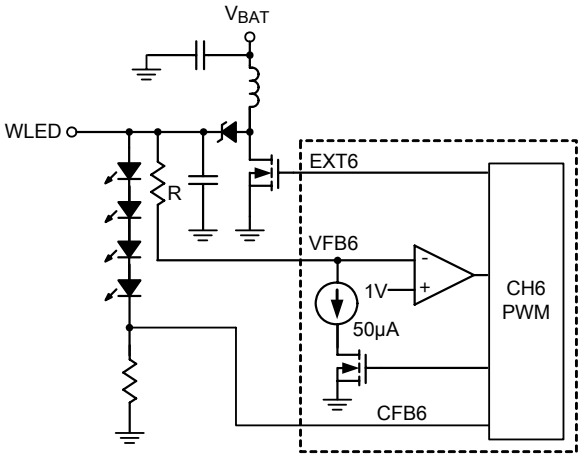



Figure 8. CH6 Over Voltage Protection Method
($V_{WLED}$ > 50µA x R+1V, protection happens)

**RT9911 Component Selection for Compensation :**

**CH1 Sync-Boost (Select Pin = High Logic) :**

CH1 sync-boost converter employs current-mode control to simplify the control loop compensation. There is a RHPZ (Right Hand Plane Zero) appeared in the loop-gain frequency response when a boost converter operates with continuous inductor current (typically the case), we also call it works in CCM (Continuous Current Mode). For stability, cross over frequency ($f_C$), unity gain frequency, must lower than this RHPZ frequency.

The fixed parameters for CH1 boost compensation are as follows :

- Transconductance (from FB to COMP), GM = 200µs
- Current sense transresistance, $R_{CS}$ = 0.4V/A
- Feedback voltage, $V_{FB}$ = FB = 0.8V

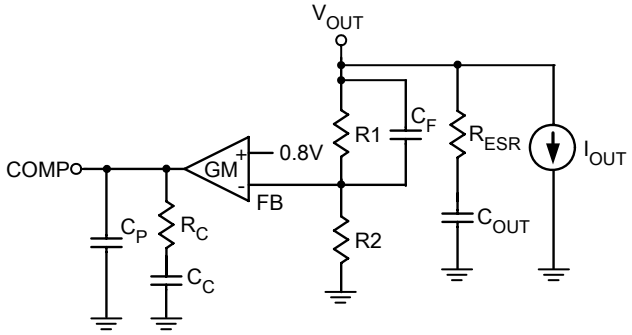



Figure 7

The input parameters for CH1 boost compensation are as follows:

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $F_{OSC}$, operating frequency
- L, inductance
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)
- $T_{DRP}$(%), Transient droop.

The results we will get for CH1 boost compensation are as follows:

- R2, the voltage divider resistor in between FB and ground.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with Rc and connect to ground.
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF).
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.

The major steps for getting above results :

1. $R2 = R1 x \left( \frac{V_{FB}}{(V_{OUT} - V_{FB})} \right)$

2. Find RHPZ(Right Hand Plan Zero) location.

$RHPZ(Boost) = R_{LOAD} x \frac{(1-D)^2}{2\pi L}$, Where

$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX.)}}, D = \text{Duty Cycle} = 1 - \frac{V_{IN}}{V_{OUT}}$

3. Set $f_C$ (cross over frequency) sufficiently below RHPZ.

For example : $f_C$ = RHPZ/6

4. Get $C_C = \left( \frac{R_{LOAD}}{R_{CS}} \right) x \frac{GM}{2\pi f_C} x \frac{V_{FB}}{V_{OUT}} x (1 - D)$

5. Select Rc based on the allowed transient droop.

$R_C = dI x (\frac{1}{(1-D)}) x \frac{R_{CS}}{GM x dV_{FB}}$

, where dI = transient step, $dV_{FB} = T_{DRP}(\%) x V_{FB}$

6. Get $C_{OUT} = \frac{R_C x C_C}{R_{LOAD}}$

7. Find ffz, zero and ffp, pole ratio of voltage divider with $C_F$.

$$ratio = \frac{ffz}{ffp} = \frac{V_{OUT}}{V_{FB}}$$

8. Get $C_F$ by placing ffp on $f_C$ and ffz therefore on $\frac{f_C}{ratio}$.

$C_f = \frac{1}{2 x \pi x ffz x R1}$, where $ffz = \frac{f_C}{ratio}$

9. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).

$C_P = C_{OUT} \frac{R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

Example : Set R1 = 470kΩ, $V_{IN}$ = 1.8V, $V_{OUT}$ = 3.3V, $V_{FB}$ = 0.8V, $I_{OUT(MAX.)}$ = 0.5A, $f_{OSC}$ = 500kHz, L = 4.7μH, $R_{ESR}$ = 5mΩ, and half-load transient droop is 5%.

Results:

1. $R2 = R1 \frac{V_{FB}}{V_{OUT} - V_{FB}} = 470k \frac{0.8}{3.3 - 0.8} = 150k\Omega$

2. $RHPZ(Boost) = R_{LOAD} \frac{(1-D)^2}{2\pi L} = 66.3kHz$, where

$R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}} = 6.6\Omega, (1-D) = \frac{V_{IN}}{V_{OUT}} = 0.54$

3. $f_C = \frac{RHPZ}{6} = 11kHz$

4. $C_C = \frac{\frac{R_{LOAD}}{R_{CS}} GM}{2\pi f_C} x \left( \frac{V_{FB}}{V_{OUT}} \right) x (1 - D) = 6.3nF.$

Choose 6.8nF.

Half-load transient means load from 0.25A to 0.5A transient. So, dI=0.5 – 0.25=0.25A

$dV_{FB} = T_{DRP}(\%) x V_{FB} = 5\% x 0.8 = 0.04V.$

Thus,

5. $R_C = \frac{dI \left( \frac{1}{(1-D)} \right) x R_{CS}}{GM x dV_{FB}} = 23k\Omega$

6. $C_{OUT} = \frac{R_C x C_C}{R_{LOAD}} = \frac{23k x 6.8n}{6.6} = 22\mu F.$

7. $ratio = \frac{ffp}{ffz} = \frac{V_{OUT}}{V_{FB}} = \frac{3.3}{0.8} = 4.1$

8. $C_F = \frac{1}{2\pi \times ffZ \times R1} = 126pF$, where

$ffZ = \frac{f_C}{ratio} = \frac{11k}{4.1} = 2.68kHz$

Choose $C_F$ = 150pF

9. $C_P = \frac{C_{OUT} x R_{ESR}}{R_C} = \frac{22\mu F x 0.005}{23k} = 4.8pF,$

which is less than 10pF. So, It can be ignored.

**CH1 Sync-Buck (Select Pin = Low Logic) and CH2 Sync-Buck :**

CH1 sync-buck (select pin=low logic) and CH2 sync-buck are converters employ current-mode control to simplify the control loop compensation. There is no RHPZ (Right Hand Plan Zero) in the buck topology but there is a high frequency pole $f_{HP}$ >= $f_{OSC}$ /π . The $f_C$ (cross over frequency) is chosen sufficient less than $f_{HP}$.

The fixed parameters for CH1 and CH2 buck compensation are as follows:

- Transconductance (from FB to COMP), GM = 200μs
- Current sense transresistance, $R_{CS}$ = 0.3V/A
- Feedback voltage, $V_{FB}$ = FB = 0.8V

The input parameters for CH1 and CH2 buck compensation are as follows:

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.

- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $f_{OSC}$, operating frequency
- L, inductance
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)
- $T_{DRP}$(%), Transient droop.

The results we will get for CH1 boost compensation are as follows:

- R2, the voltage divider resistor in between FB and ground.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.

The major steps for getting above results :

1. $R2 = R1\frac{V_{FB}}{V_{OUT} - V_{FB}}$
2. Set fc (cross over frequency) sufficiently below $f_{OSC}$.

For example : $f_C = \frac{f_{HP}}{4}$

3. $C_C = \frac{R_{LOAD}}{R_{CS}} \times \frac{GM}{2\pi f_C} \times \frac{V_{FB}}{V_{OUT}}$

4. $R_C = \frac{dI \times R_{CS}}{GM \times dV_{FB}}$, where dI = transient step,
   $dV_{FB} = T_{DRP}(\%) \times V_{FB}$
5. Get $C_{OUT} = \frac{R_C \times C_C}{R_{LOAD}}$
6. Find ffz, zero and ffp, pole ratio of voltage divider with $C_F$.
   $ratio = \frac{ffp}{ffz} = \frac{V_{OUT}}{V_{FB}}$
7. Get $C_F$ by placing ffp on $f_C$ and ffz therefore on $\frac{f_C}{ratio}$.
   $C_F = \frac{1}{2\pi \times ff_Z \times R1}$, where $ff_Z = \frac{f_C}{ratio}$.
8. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).
   $C_P = \frac{C_{OUT} \times R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

Example : Set R1 = 470kΩ, $V_{IN}$ = 3V, $V_{OUT}$ = 1.8V, $V_{FB}$ = 0.8V, $I_{OUT(MAX.)}$ = 0.5A, $f_{OSC}$ = 500kHz, L = 4.7μH, $R_{ESR}$ = 5mΩ, and half-load transient droop is 5%.

Results :

1. $R2 = R1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}} = 470k \times \frac{0.8}{1.8 - 0.8} = 376k\Omega$

2. $f_C = \frac{f_{HP}}{4} = \frac{f_{OSC}}{4\pi} = 40kHz$

3. $C_C = \frac{R_{LOAD}}{R_{CS}} \times \frac{GM}{2\pi f_C} \times \frac{V_{FB}}{V_{OUT}} = 4.25nF$, where
   $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX.)}} = 3.6\Omega$

   Choose 4.7nF.

   Half-load transient means load from 0.25A to 0.5A transient. So, dI = 0.5 – 0.25=0.25A

   $dV_{FB} = T_{DRP}(\%) \times V_{FB} = 5\% \times 0.8 = 0.04V$.

Thus,

4. $R_C = dI \frac{R_{CS}}{GM \times dV_{FB}} = 9.4k\Omega$, choose 10kΩ.

5. $C_{OUT} = \frac{R_C \times C_C}{R_{LOAD}} = \frac{10k \times 3.9nF}{3.6} = 10.8\mu F$. Choose 10μF.

6. $ratio = \frac{ffp}{ffz} = \frac{V_{OUT}}{V_{FB}} = \frac{1.8}{0.8} = 2.25$

7. $C_F = \frac{1}{2\pi \times ff_Z \times R1} = 15.2pF$, where
   $ff_Z = \frac{f_C}{ratio} = \frac{50k}{2.25} = 22.2kHz$

   Choose $C_F$ = 22pF

8. $C_P = \frac{C_{OUT} \times R_{ESR}}{R_C} = \frac{10\mu \times 0.005}{10k} = 5pF$,
   which is less than 10pF. So, It can be ignored.

**CH3 Syn Boost Controller with External MOSFET :**

CH3 boost controller driving external logic level MOSFET employs current-mode control to simplify the control loop compensation. There is a RHPZ (Right Hand Plan Zero) appeared in the loop-gain frequency response when a boost converter operates with continuous inductor current (typically the case), we also call it works in CCM (Continuous Current Mode). For stability, cross over frequency ($f_C$), unity gain frequency, must lower than this RHPZ frequency.

The fixed parameters for CH3 boost compensation are as follows :

- Transconductance (from FB to COMP), GM = 200μs
- Feedback voltage, $V_{FB}$ = FB = 0.8V

The input parameters for boost compensation are as follows :

- $R_{DS(ON)}$, the NMOSFET $R_{DS(ON)}$, which is use to find transresistance, $R_{CS}$.
- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $F_{OSC}$, operating frequency
- L, inductance
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)
- $T_{DRP}$(%), Transient droop.

The results we will get for boost compensation are as follows :

- $R_{CS}$, the transresistance of current sense.
- R2, the voltage divider resistor in between FB and ground.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.

The major steps for getting above results :

1. $R_{CS} = 2 \times R_{DS(ON)}$

The rest of the steps are the same as sync-boost.

**CH4 Asyn-Boost Controller with External MOSFET**

CH4 is an asyn-boost controller driving external logic level N type MOSFET, which employs voltage mode control to regulate the output voltage. Compensation depends on designing the loading range working in discontinuous or continuous inductor current mode. (DCM or CCM).

**Asyn-Boost in DCM :**

We call it DCM because inductor current falls to zero on each switch cycle. The benefit of designing in DCM is the simple loop compensation, which has no RHPZ (Right Hand Plan Zero) and conjugate double pole in the frequency domain to worry about, but has a single load pole instead. However, the output ripple and efficiency are worse than in CCM (Continuous Inductor Current). If the loading is around tens of mA, it is not bad to design in DCM with less impact on the output ripple and efficiency, but gain more easy to stabilize the control loop.

The fixed parameters for CH4 asyn-boost in DCM compensation are as follows:

- Transconductance (from FB to COMP), GM = 200us.
- Internal voltage ramp to decide duty cycle, $V_P$ = 1V.
- Feedback voltage, $V_{FB}$ = FB = 1V

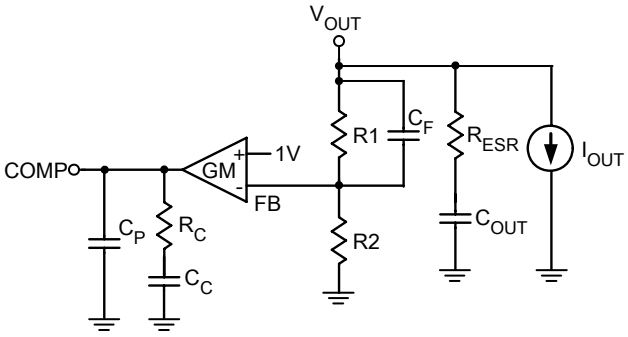



Figure 9

The input parameters for CH4 asyn-boost in DCM compensation are as follows :

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $f_{OSC}$, operating frequency
- L, inductance
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)

The results we will get for CH4 asyn-boost in DCM compensation are as follows :

- R2, the voltage divider resistor in between FB and ground.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)

The major steps for getting above results :

1. $R2 = R1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$
2. Select suitable inductor to ensure $I_{OUT(MIN.)}$ works in DCM, which is let inductor current falls to zero on each switch cycle.
   $L < \frac{V_{IN} \times D \times (1-D)}{2 \times I_{OUT(MAX.)} \times f_{OSC}}$
3. Set $f_C$ sufficient below $f_{OSC}$.

For example: $f_C = \frac{f_{OSC}}{10}$ or lower

4. Find the load pole : $f_{LP} = \frac{2 \times M - 1}{2\pi \times (M-1) \times R_{LOAD} \times C_{OUT}}$,
   where $M = \frac{V_{OUT}}{V_{IN}}$, $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX.)}}$.
5. Get $R_C = \frac{\frac{f_C}{f_{LP}} \times V_P}{GM \times G_{dod}}$, where $G_{dod} = 2 \times \frac{V_{OUT}}{D} \times \frac{M-1}{2 \times M - 1}$,
   which is duty to $V_{OUT}$ transfer function.
   $D = \text{duty cycle} = 1 - \frac{V_{IN}}{V_{OUT}}$
6. Get $C_C = C_{OUT} \times \frac{R_{LOAD}}{R_C}$
   by letting comp zero = load pole.
7. Find ffz, zero and ffp, pole ratio of voltage divider with $C_F$.
   $\text{ratio} = \frac{ffp}{ffz} = \frac{V_{OUT}}{V_{FB}}$
8. Get $C_F$ by placing ffp on $f_C$ and ffz therefore on $\frac{f_C}{\text{ratio}}$.
   $C_F = \frac{1}{2\pi \times ff_Z \times R1}$, where $ff_Z = \frac{f_C}{\text{ratio}}$.
9. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).
   $C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

**Asyn-boost in CCM :**

We call it CCM because inductor current is always continuous in operation. The benefit of designing in CCM is lower $V_{OUT}$ and inductor current ripple and higher efficiency from the lower coil loss, but with the expense of larger inductor size and cost and the control loop comes with a RHPZ (Right Hand Plan Zero) and a conjugate double pole in the frequency domain to worry about.

The fixed parameters for CH4 asyn-boost in CCM compensation are as follows :

- Transconductance (from FB to COMP), GM = 200µs
- Internal voltage ramp to decide duty cycle, $V_P$ = 1V
- Feedback voltage, $V_{FB}$ = FB = 1V

The input parameters for CH4 asyn-boost in CCM compensation are as follows :

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $I_{OUT(MIN.)}$, minimum output laod
- $f_{OSC}$, operating frequency

- L, inductance
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)

The results we will get for CH4 asyn-boost in CCM compensation are as follows:

- R2, the voltage divider resistor in between FB and ground.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)

The major steps for getting above results :

1. $R2 = R1 \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$
2. Select suitable inductor to ensure $I_{OUT(MIN.)}$ works in CCM,
   $L > \frac{V_{IN} \times D \times (1-D)}{2 \times I_{OUT(MIN.)} \times f_{OSC}}$
3. Find RHPZ(Right Hand Plan Zero) location.
   $RHPZ(Boost) = R_{LOAD} \frac{(1-D)^2}{2\pi L}$, where
   $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}}$, $D = \text{duty cycle} = 1 - \frac{V_{IN}}{V_{OUT}}$
4. Set $f_C$ (cross over frequency) sufficiently below RHPZ.
   For example : $f_C = \frac{RHPZ}{6}$ or lower.
5. Find the load pole : $f_{LP} = \frac{2 \times M - 1}{2\pi \times (M-1) \times R_{LOAD} \times C_{OUT}}$,
   where $M = \frac{V_{OUT}}{V_{IN}}$, $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX.)}}$.
6. Get $R_C = \frac{\frac{f_C}{f_{LP}} \times V_P}{GM \times G_{doc}}$, where $G_{doc} = \frac{V_{IN}}{(1-D)^2}$,
   which is duty to $V_{OUT}$ transfer function.
   $D = \text{duty cycle} = 1 - \frac{V_{IN}}{V_{OUT}}$.
7. Find $f_{cdp} = \frac{1-D}{2\pi \times (LC)^2}$,
   which is the conjugate double pole from LC filter.
8. $C_C = \frac{1}{2\pi \times f_{cdp} \times R_C}$ to cancel one of the double pole.
9. Find $C_f$ by placing its zero on $f_{cdp}$ to cancel another double pole.
   $C_F = \frac{1}{2\pi \times f_{cdp} \times R1}$.
10. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).
    $C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

**CH5 Asyn-Inverter Controller with External MOSFET**

CH5 is an asyn-inverter controller driving external logic level P type MOSFET, which employs voltage mode control to regulate the output voltage. Compensation depends on designing the loading range working in discontinuous or continuous inductor current mode. (DCM or CCM).

**Asyn-Inverter in DCM :**

We call it DCM because inductor current falls to zero on each switch cycle. The benefit of designing in DCM is the simple loop compensation, which has no RHPZ (Right Hand Plan Zero) and conjugate double pole in the frequency domain to worry about, but has a single load pole instead. However, the output ripple and efficiency are worse than in CCM (Continuous Inductor Current). If the loading is around tens of mA, it is not bad to design in DCM with less impact on the output ripple and efficiency, but gain more easy to stabilize the control loop.

The fixed parameters for CH5 asyn-inverter in DCM compensation are as follows:

- Transconductance (from FB to COMP), GM = 200μs
- Internal voltage ramp to decide duty cycle, $V_P$ = 1V
- Feedback voltage, $V_{FB}$ = FB = 0V
- Reference voltage, $V_{REF}$ = 1V

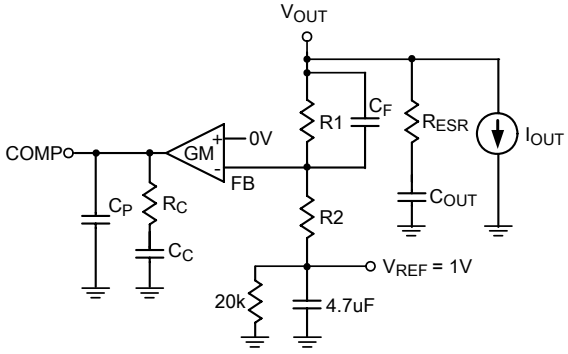



Figure 10

The input parameters for CH5 asyn-inverter in DCM compensation are as follows :

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load
- $f_{OSC}$, operating frequency
- L, inductance
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)

The results we will get for CH5 asyn-inverter in DCM compensation are as follows :

- R2, the voltage divider resistor in between FB and $V_{REF}$.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)

The major steps for getting above results :

1. $R2 = R1 \times \frac{V_{REF} - V_{FB}}{V_{FB} - V_{OUT}}$. If $R1 = 1M\Omega$ and $V_{OUT} = (-8)V$

   then $R2 = 1M \times \frac{1-0}{0-(-8)} = 125k\Omega$

2. Select suitable inductor to ensure $I_{OUT(MIN.)}$ works in DCM, which is let inductor current falls to zero on each switch cycle.

   $$L < \frac{V_{IN} \times (1-D)}{2 \times I_{OUT(MAX.)} \times f_{OSC}}$$

3. Set $f_C$ sufficient below $f_{OSC}$

   For example: $f_C = \frac{f_{OSC}}{10}$ or lower

4. Find the load pole : $f_{LP} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}$,

   where $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX.)}}$.

5. Get $R_C = \frac{\frac{f_C}{f_{LP}} \times V_P}{GM \times G_{dod}}$, where $G_{dod} = \frac{V_{OUT}}{D}$,

   which is duty to Vout transfer function.

   $D = \text{duty cycle} = \frac{abs(V_{OUT})}{V_{IN} + abs(V_{OUT})}$.

6. Get $C_C = C_{OUT} \times \frac{R_{LOAD}}{R_C}$

   by letting comp zero = load pole.

7. Find ffz, zero and ffp, pole ratio of voltage divider with $C_F$.

   $ratio = \frac{ffp}{ffz} = \frac{abs(V_{OUT}) + V_{REF}}{V_{REF}}$

8. Get $C_F$ by placing ffp on $f_C$ and ffz therefore on $\frac{f_C}{ratio}$.

   $C_F = \frac{1}{2\pi \times ffz \times R1}$, where $ffz = \frac{f_C}{ratio}$.

9. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).

   $C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

**Asyn-Inverter in CCM :**

We call it CCM because inductor current is always continuous in operation. The benefit of designing in CCM is lower $V_{OUT}$ and inductor current ripple and higher efficiency from the lower coil loss, but with the expense of larger inductor size and cost and the control loop comes with a RHPZ (Right Hand Plan Zero) and a conjugate double pole in the frequency domain to worry about.

The fixed parameters for CH5 asyn-inverter in CCM compensation are as follows :

- Transconductance (from FB to COMP), GM = 200us
- Internal voltage ramp to decide duty cycle, $V_P$ = 1V
- Feedback voltage, $V_{FB}$ = FB = 0V
- Reference voltage, $V_{REF}$ = 1V

The input parameters for CH5 asyn-inverter in CCM compensation are as follows :

- R1, the voltage divider resistor in between $V_{OUT}$ and FB.
- $V_{IN}$, input voltage.
- $V_{OUT}$, desired output voltage
- $I_{OUT(MAX.)}$, maximum output load

- $I_{OUT(MIN.)}$, minimum output laod
- $f_{OSC}$, operating frequency
- L, inductance
- $C_{OUT}$, output capacitance. This compensation is based on ceramic output capacitor.
- $R_{ESR}$, ESR (Equivalent Series Resistance) of $C_{OUT}$ (ceramic output capacitor)

The results we will get for CH5 asyn-inverter in CCM compensation are as follows :

- R2, the voltage divider resistor in between FB and $V_{REF}$.
- $C_F$, feedforward capacitor in parallel with R1.
- $R_C$, compensation resistor on COMP pin.
- $C_C$, compensation capacitor in series with $R_C$ and connect to ground
- $C_P$, connect in between COMP pin and ground. (Can be ignored if $C_P$ < 10pF)

The major steps for getting above results :

1. $R2 = R1 \times \frac{V_{REF} - V_{FB}}{V_{FB} - V_{OUT}}$. If $R1 = 1M\Omega$ and $V_{OUT} = (-8)V$

   then $R2 = 1M \times \frac{1-0}{0-(-8)} = 125k\Omega$

2. Select suitable inductor to ensure $I_{OUT(MIN.)}$ works in CCM,

   $L < \frac{V_{IN} \times (1-D)}{2 \times I_{OUT(MIN.)} \times f_{OSC}}$

3. Find RHPZ(Right Hand Plan Zero) location.

   $RHPZ(Boost) = R_{LOAD} \frac{\frac{(1-D)^2}{D}}{2\pi L}$, where

   $R_{LOAD} = \frac{V_{OUT}}{I_{OUT(MAX)}}$, $D = \text{duty cycle} = \frac{abs(V_{OUT})}{V_{IN} + abs(V_{OUT})}$

4. Set $f_C$ (cross over frequency) sufficiently below RHPZ.

   For example: $f_C = \frac{RHPZ}{6}$ or lower

5. Find the load pole : $f_{LP} = \frac{2}{2\pi \times R_{LOAD} \times C_{OUT}}$,

   where $R_{LOAD} = \frac{abs(V_{OUT})}{I_{OUT(MAX.)}}$.

6. Get $R_C = \frac{\frac{f_C}{f_{LP}} \times V_P}{GM \times G_{doc}}$, where $G_{doc} = \frac{V_{IN}}{(1-D)^2}$,

   which is duty to $V_{OUT}$ transfer function.

   $D = \text{duty cycle} = \frac{abs(V_{OUT})}{V_{IN} + abs(V_{OUT})} V_{OUT}$

7. Find $f_{cdp} = \frac{1-D}{2\pi \times (LC)^2}$,

   which is the conjugate double pole from LC filter.

8. $C_C = \frac{1}{2\pi \times f_{cdp} \times R_C}$ to cancel one of the double pole.

9. Find $C_f$ by placing its zero on fcdp to cancel another double pole.

   $C_F = \frac{1}{2\pi \times f_{cdp} \times R1}$.

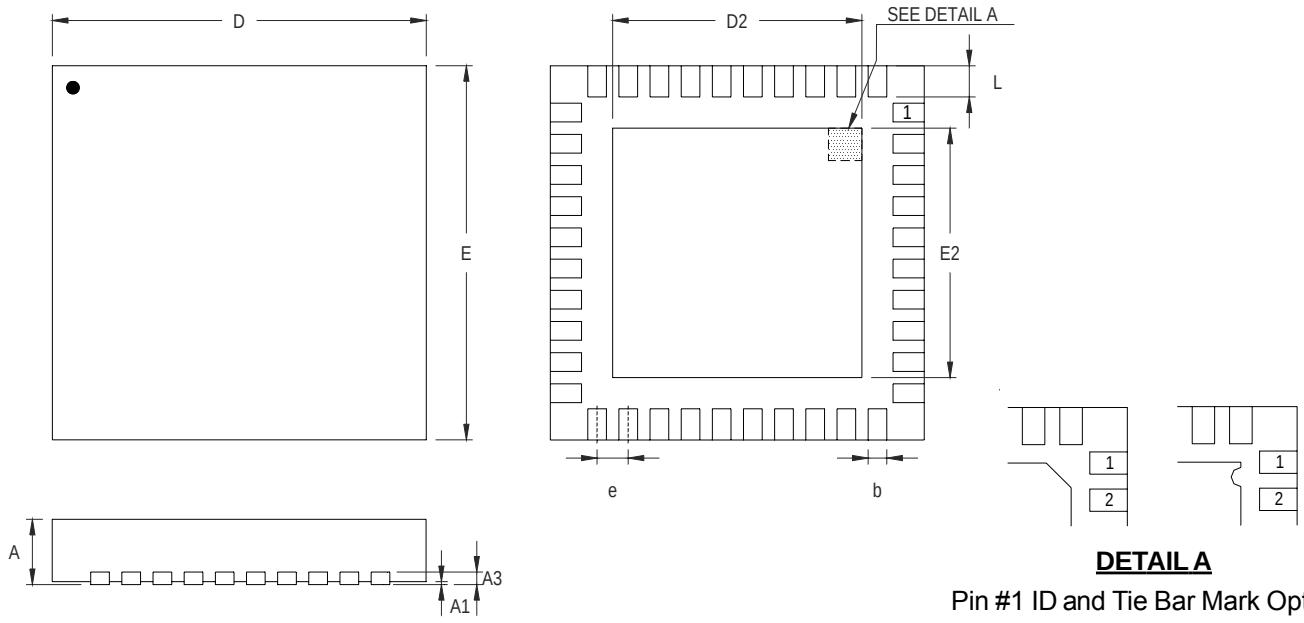
10. Evaluate $C_P$. $C_P$ is for canceling the zero from $C_{OUT}$ (ceramic output capacitor).

    $C_P = C_{OUT} \times \frac{R_{ESR}}{R_C}$. $C_P$ can be ignore if $C_P < 10pF$.

**PCB Layout Considerations**

- The feedback netwok should be very close to the FB pin.
- The compensation network should be very close to the COMP pin and avoid through VIA.
- For CH3 current sense, CS should be close to the drain site of external NMOS.
- Keep high current path as short as possible.

## Outline Dimension




**DETAIL A**

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.800 | 1.000 | 0.031 | 0.039 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A3 | 0.175 | 0.250 | 0.007 | 0.010 |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| D | 5.950 | 6.050 | 0.234 | 0.238 |
| D2 | 4.000 | 4.750 | 0.157 | 0.187 |
| E | 5.950 | 6.050 | 0.234 | 0.238 |
| E2 | 4.000 | 4.750 | 0.157 | 0.187 |
| e | 0.500 | | 0.020 | |
| L | 0.350 | 0.450 | 0.014 | 0.018 |

**V-Type 40L QFN 6x6 Package**

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