PCA2125

SPI Real-time clock/calendar

Rev. 01 — 28 July 2008 Product data sheet

1. General description

The PCA2125 is a CMOS real-time clock/calendar optimized for low-power consumption and an operating temperature up to 125 °C. Data is transferred via a Serial Peripheral Interface (SPI) bus with a maximum data rate of 6.0 Mbit/s. An alarm and timer function are also available with the possibility to generate a wake-up signal on an interrupt pin.

AEC Q100 qualified for automotive applications.

2. Features

- Provides year, month, day, weekday, hours, minutes and seconds based on 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.3 V to 5.5 V
- Low backup current: typical 0.55 µA at V_{DD} = 3.0 V and T_{amb} = 25 °C
- 3-line SPI-bus with separate combinable data input and output
- Serial interface (at V_{DD} = 1.6 V to 5.5 V)
- 1 second or 1 minute interrupt output
- Freely programmable timer with interrupt capability
- Freely programmable alarm function with interrupt capability
- Integrated oscillator capacitor
- Internal power-on reset
- Open-drain interrupt pin

3. Applications

- Automotive time keeping application
- Metering

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA2125TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

5. Marking

Table 2. Marking codes

Type number	Marking code
PCA2125TS	PCA2125

6. Block diagram

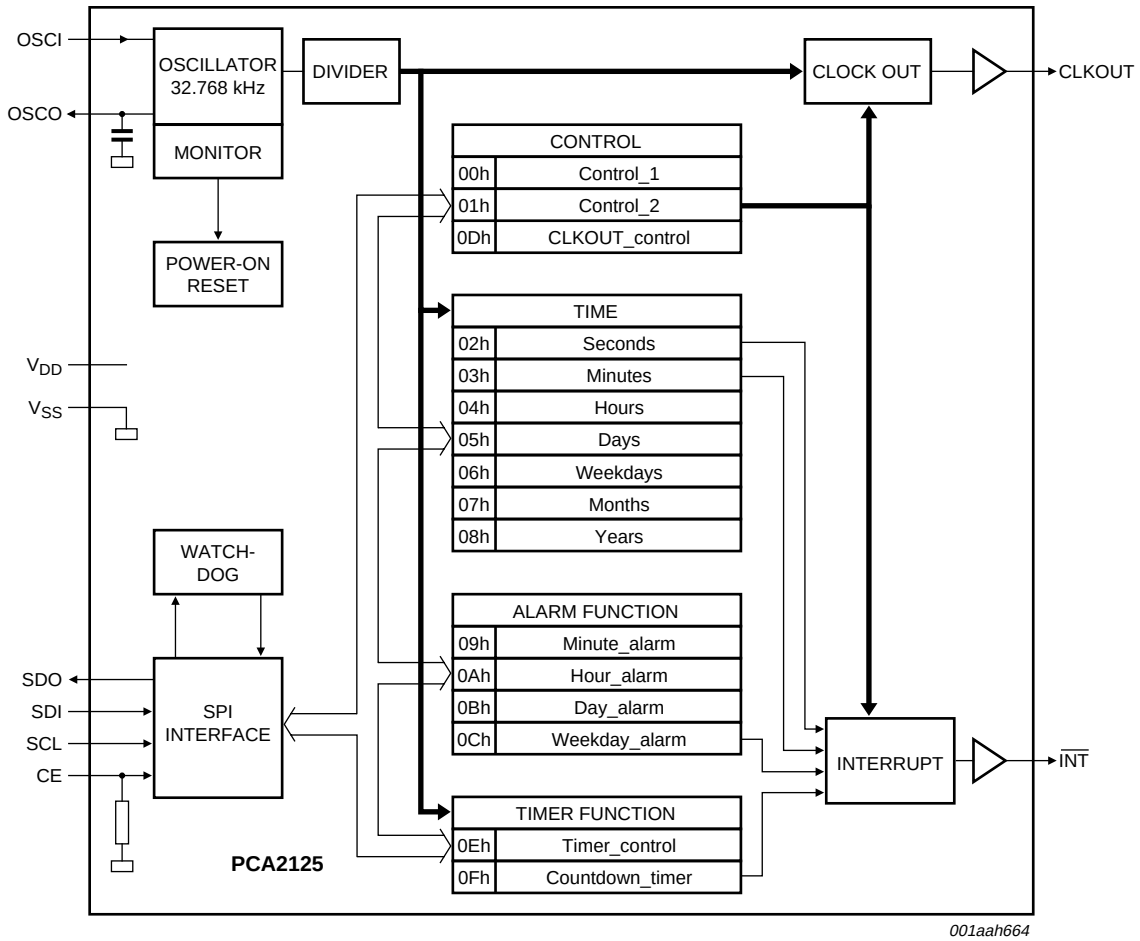


Fig 1. Block diagram of PCA2125

7. Pinning information

7.1 Pinning

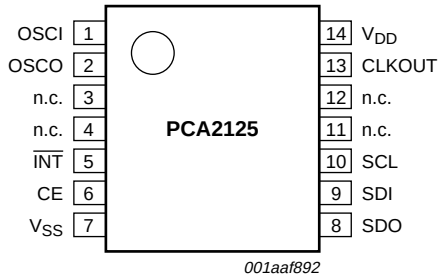


Fig 2. Pin configuration for TSSOP14

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
n.c.	3, 4	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
$\overline{INT}$	5	interrupt output (open-drain; active LOW)
CE	6	chip enable input (active HIGH) with 200 kΩ pull-down resistor
V_{SS}	7	ground
SDO	8	serial data output, push-pull
SDI	9	serial data input; might float when CE inactive
SCL	10	serial clock input; might float when CE inactive
n.c.	11, 12	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
CLKOUT	13	clock output (open-drain)
V_{DD}	14	supply voltage

8. Functional description

The PCA2125 contains sixteen 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the Real-Time Clock (RTC), a programmable clock output, and a 6 MHz SPI-bus.

All sixteen registers are designed as addressable 8-bit parallel registers although not all bits are implemented:

- The first two registers at addresses 00h and 01h (Control_1 and Control_2) are used as control registers.
- Registers at addresses 02h to 08h (Seconds, Minutes, Hours, Days, Weekdays, Months, Years) are used as counters for the clock function. Seconds, minutes, hours, days, months and years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is read the contents of all counters are frozen. Therefore, faulty reading of the clock/calendar during a carry condition is prevented.
- Registers at addresses 09h to 0Ch (Minute_alarm, Hour_alarm, Day_alarm, Weekday_alarm) define the alarm condition.
- Register at address 0Dh (CLKOUT_control) defines the clock out mode.
- Registers at addresses 0Eh and 0Fh (Timer_control and Countdown_timer) are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

8.1 Register overview

The time registers are encoded in BCD to simplify application use. Other registers are either bit-wise or standard binary.

Table 4. Register overview

Bits labeled '-' are not implemented and will return a logic 0 when read. Bit positions labeled '0' should always be written with logic 0.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	EXT_TEST	0	STOP	0	POR_OVRD	12_24	0	0
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
02h	Seconds	RF	SECONDS[1]			SECONDS			
03h	Minutes	-	MINUTES[1]			MINUTES			
04h	Hours	-	-	AMPM	HOURS[1]	HOURS			
		-	-	HOURS[2]		HOURS			
05h	Days	-	-	DAYS[1]		DAYS			
06h	Weekdays	-	-	-	-	-	WEEKDAYS		
07h	Months	-	-	-	MONTHS[1]	MONTHS			
08h	Years	YEARS[1]				YEARS			
09h	Minute_alarm	AEN_M	MINUTE_ALARM[1]			MINUTE_ALARM			
0Ah	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM[1]	HOUR_ALARM			
			-	HOUR_ALARM[2]		HOUR_ALARM			
0Bh	Day_alarm	AEN_D	-	DAY_ALARM[1]		DAY_ALARM			
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM		
0Dh	CLKOUT_control	-	-	-	-	-	COF		
0Eh	Timer_control	TE	-	-	-	-	-	CTD	
0Fh	Countdown_timer	COUNTDOWN_TIMER							

[1] Ten's place.

[2] Ten's place in 24 h mode.

8.2 Reset

The PCA2125 includes an internal reset circuit which is active whenever the oscillator is stopped; see Figure 3. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground.

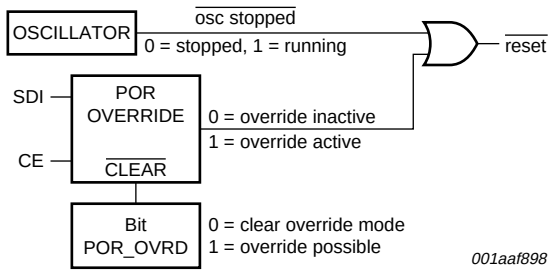


Fig 3. Reset system

The oscillator is considered to be stopped during the time between power-up and stable crystal resonance; see Figure 4. This time can be in the range 200 ms to 2 s depending on crystal type, temperature and supply voltage. Whenever an internal reset occurs, the reset flag bit RF is set.

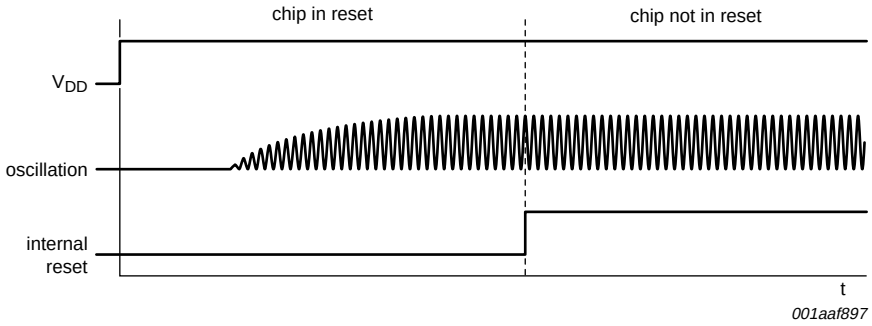


Fig 4. Power-on reset

Table 5. Register reset value

Bits labeled '-' are not implemented and will return a '0' when read. Bits labeled 'X' are undefined at power-up and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	-	1	0	-	-
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	-	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X

Table 5. Register reset value *…continued*

Bits labeled '-' are not implemented and will return a '0' when read. Bits labeled 'X' are undefined at power-up and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
07h	Months	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute_alarm	1	X	X	X	X	X	X	X
0Ah	Hour_alarm	1	-	X	X	X	X	X	X
0Bh	Day_alarm	1	-	X	X	X	X	X	X
0Ch	Weekday_alarm	1	-	-	-	-	X	X	X
0Dh	CLKOUT_control	-	-	-	-	-	0	0	0
0Eh	Timer_control	0	-	-	-	-	-	1	1
0Fh	Countdown_timer	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- Power-on reset override available to be set
- 24 hour mode is selected

The SPI-bus is initialized whenever the chip enable pin CE is inactive (LOW).

8.2.1 Power-on reset override

The Power-On Reset (POR) duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up the on-board test of the device.

The setting of this mode requires that bit POR_OVRD be set to logic 1 and that the signals at the SPI-bus pins SDI and CE are toggled as illustrated in Figure 5. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and set-up operation can commence i.e. entry into the external clock test mode via the SPI-bus access. The override mode can be cleared by writing a logic 0 to bit POR_OVRD. Bit POR_OVRD must be set to logic 1 before a re-entry into the override mode is possible. Setting bit POR_OVRD to logic 0 during normal operation has no effect except to prevent accidental entry into the POR override mode. This is the recommended setting.

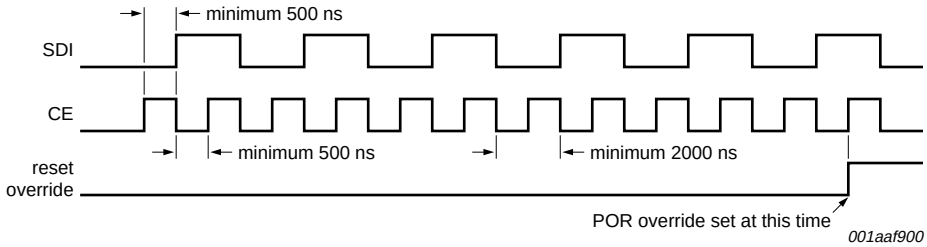


Fig 5. POR override sequence

8.3 Control registers

Table 6. Control_1 register (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0	normal mode	Section 8.9
		1	external clock test mode	
6	-	0	unused	
5	STOP	0	RTC source clock runs	Section 8.10
		1	RTC divider chain flip-flops are asynchronously set to logic 0; the RTC clock is stopped (CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available)	
4	-	0	unused	-
3	POR_OVRD	0	power-on reset override facility is disabled; **set to logic 0 for normal operation**	Section 8.2.1
		1	power-on reset override is enabled	
2	12_24	0	24 hour mode is selected	Table 11
		1	12 hour mode is selected	
1 to 0	-	0	unused	-

Table 7. Control_2 register (address 01h) bit description

Bit	Symbol	Value	Description	Reference
7	MI	0	minute interrupt is disabled	Section 8.6.1
		1	minute interrupt is enabled	
6	SI	0	second interrupt is disabled	
		1	second interrupt is enabled	
5	MSF	0	no minute or second interrupt generated	Section 8.6
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt	
4	TI_TP	0	interrupt pin follows timer flags	Section 8.7.2
		1	interrupt pin generates a pulse	
3	AF	0	no alarm interrupt generated	Section 8.5.1
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
2	TF	0	no countdown timer interrupt generated	-
		1	flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt	-
1	AIE	0	no interrupt generated from the alarm flag	Section 8.7.3
		1	interrupt generated when alarm flag set	
0	TIE	0	no interrupt generated from the countdown timer flag	Section 8.7
		1	interrupt generated when countdown timer flag set	

8.4 Time and date function

The majority of the registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use.

An example is shown for register Minutes in Table 8.

Table 8. BCD example

Minutes value (decimal)	Double-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	2^3	2^2	2^1	2^0	2^3	2^2	2^1	2^0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

Table 9. Register Seconds (address 02h) bit description

Bit	Symbol	Value	Description
7	RF	0	clock integrity is guaranteed
		1	clock integrity is not guaranteed; chip reset has occurred since flag was last cleared
6 to 0	SECONDS[6:0]	00 to 59	this register holds the current seconds value coded in BCD format

Table 10. Register Minutes (address 03h) bit description

Bit	Symbol	Value	Description
7	-	0	unused
6 to 0	MINUTES[6:0]	00 to 59	this register holds the current minutes value coded in BCD format

Table 11. Register Hours (address 04h) bit description

Bit	Symbol	Value	Description
6 and 7	-	0	unused
12 hour mode[1]			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	HOURS[4:0]	01 to 12	this register holds the current hours value coded in BCD format for 12 hour mode
24 hour mode[1]			
5 to 0	HOURS[5:0]	00 to 23	this register holds the current hours value coded in BCD format for 24 hour mode

[1] Hour mode is set by bit 12_24 in register Control_1.

Table 12. Register Days (address 05h) bit description

Bit	Symbol	Value	Description
6, 7	-	0	unused
5 to 0	DAYS[5:0]	01 to 31	this register holds the current day value coded in BCD format[1]

[1] The RTC compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

Table 13. Register Weekdays (address 06h) bit description

Bit	Symbol	Value	Description
3 to 7	-	0	unused
2 to 0	WEEKDAYS[2:0]	0 to 6	this register holds the current weekday value; see Table 14

Table 14. Weekday assignments

Day[1]	Double-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sunday	X	X	X	X	X	0	0	0
Monday	X	X	X	X	X	0	0	1
Tuesday	X	X	X	X	X	0	1	0
Wednesday	X	X	X	X	X	0	1	1
Thursday	X	X	X	X	X	1	0	0
Friday	X	X	X	X	X	1	0	1
Saturday	X	X	X	X	X	1	1	0

[1] The weekday assignments can be re-defined by the user.

Table 15. Register Months (address 07h) bit description

Bit	Symbol	Value	Description
5 to 7	-	0	unused
4 to 0	MONTHS[4:0]	01 to 12	this register holds the current month value coded in BCD format; see Table 16

Table 16. Month assignments

Month	Double-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	X	X	X	0	0	0	0	1
February	X	X	X	0	0	0	1	0
March	X	X	X	0	0	0	1	1
April	X	X	X	0	0	1	0	0
May	X	X	X	0	0	1	0	1
June	X	X	X	0	0	1	1	0
July	X	X	X	0	0	1	1	1
August	X	X	X	0	1	0	0	0
September	X	X	X	0	1	0	0	1

Table 16. Month assignments *...continued*

Month	Double-digit				Digit			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
October	X	X	X	1	0	0	0	0
November	X	X	X	1	0	0	0	1
December	X	X	X	1	0	0	1	0

Table 17. Register Years (address 08h) bit description

Bit	Symbol	Value	Description
7 to 0	YEARS[7:0]	00 to 99	this register holds the current year value coded in BCD format

Figure 6 shows the data flow and data dependencies starting from the 1 Hz clock tick.

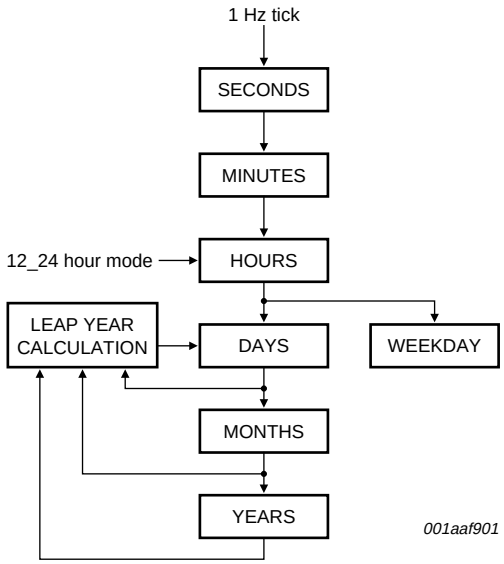


Fig 6. Data flow for the time function

8.5 Alarm function

When one or several alarm registers are loaded with a valid minute, hour, day or weekday value and its corresponding alarm enable not bit (AENx) is logic 0, then that information is compared with the current minute, hour, day and weekday value.

Table 18. Register Minute_alarm (address 09h) bit description

Bit	Symbol	Value	Description
7	AEN_M	0	minute alarm is enabled
		1	minute alarm is disabled
6 to 0	MINUTE_ALARM[6:0]	00 to 59	this register holds the minute alarm value coded in BCD format

Table 19. Register Hour_alarm (address 0Ah) bit description

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1	hour alarm is disabled
6	-	0	unused
12 hour mode			
5	AMPM	0	indicates AM
		1	indicates PM
4 to 0	HOUR_ALARM	01 to 12	this register holds the hour alarm value coded in BCD format when in 12 hour mode
24 hour mode			
5 to 0	HOUR_ALARM	00 to 23	this register holds the hour alarm value coded in BCD format when in 24 hour mode

Table 20. Register Day_alarm (address 0Bh) bit description

Bit	Symbol	Value	Description
7	AEN_D	0	day alarm is enabled
		1	day alarm is disabled
6	-	0	unused
5 to 0	DAY_ALARM	01 to 31	this register holds the day alarm value coded in BCD format

Table 21. Register Weekday_alarm (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1	weekday alarm is disabled
3 to 6	-	0	unused
2 to 0	WEEKDAY_ALARM	0 to 6	this register holds the weekday alarm value

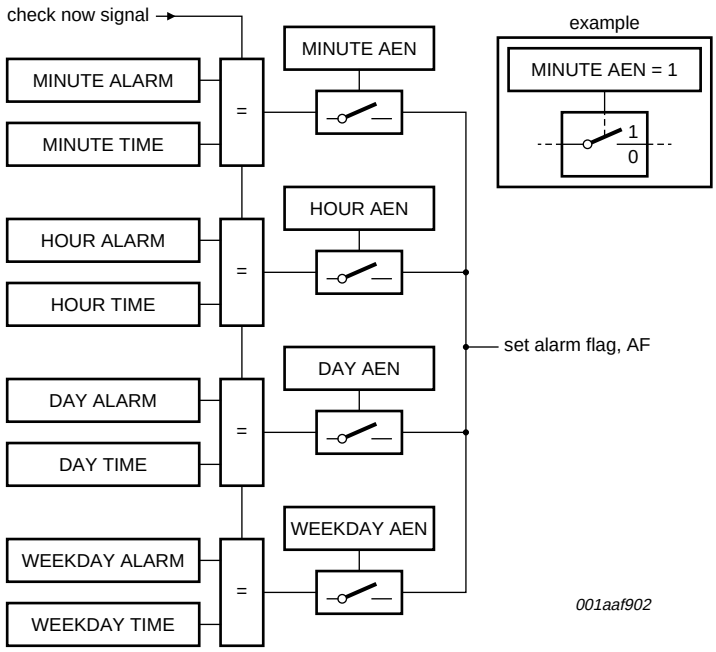


Fig 7. Alarm function block diagram

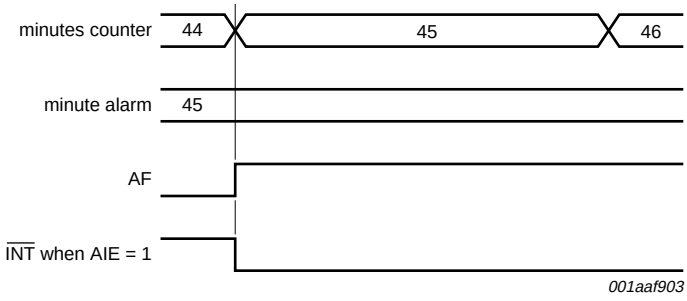
Generation of interrupts from the alarm function is described in Section 8.7.3.

8.5.1 Alarm flag

When all enabled comparisons first match, the alarm flag bit AF is set. Bit AF will remain set until cleared by software. Once bit AF has been cleared it will only be set again when the time increments once more to match the alarm condition.

Alarm registers which have their bit AENx at logic 1 are ignored.

Figure 8 shows an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 8. Alarm flag timing

To prevent the timer flags being overwritten while clearing bit AF, a logic AND is performed during a write access. The flag is reset by writing a logic 0 but its value is not affected by writing a logic 1.

Table 22. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 23 shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 23. Example to clear only AF (bit 3) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	0	1	-	-

8.6 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute.

Registers Control_2 (01h), Timer_control (0Eh) and Countdown_timer (0Fh) are used to control the timer function and output.

Table 24. Register Timer_control (address 0Eh) bit description

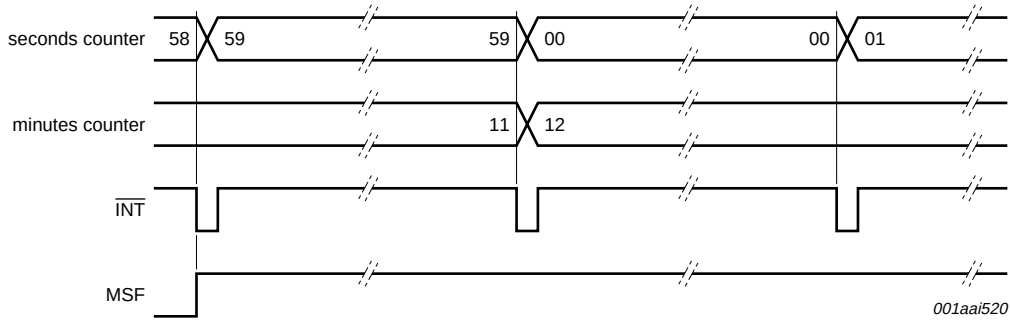
Bit	Symbol	Value	Description	Reference
7	TE	0	countdown timer is disabled	Section 8.6.2
		1	countdown timer is enabled	
6 to 2	-	0	unused	
1 to 0	CTD[1:0]	00	4096 Hz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11	$^1/_{60}$ Hz countdown timer source clock	

Table 25. Register Countdown_timer (address 0Fh) bit description

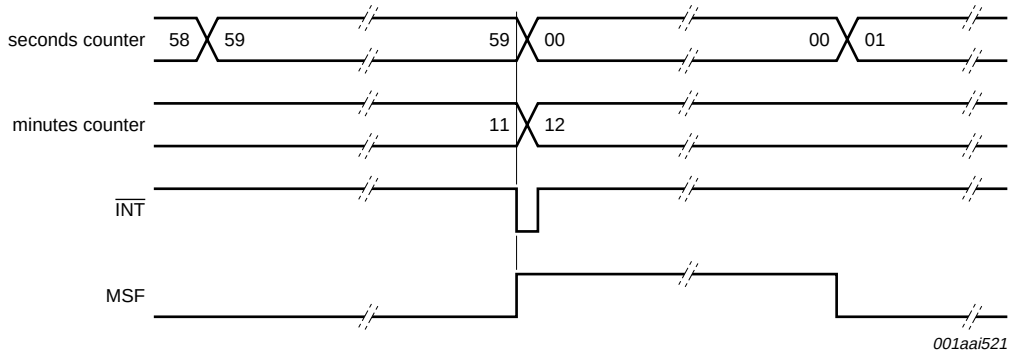
Bit	Symbol	Value	Description	Reference
7 to 0	COUNTDOWN_TIMER[7:0]	00h to FFh	countdown value = n. $CountdownPeriod = \frac{n}{SourceClockFrequency}$	Section 8.6.2

8.6.1 Second and minute interrupt

The second and minute interrupts (bits SI and MI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently of one another, however a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 9.



a. $\overline{INT}$ and MSF when SI enabled (MSF flag not cleared after an interrupt)



b. $\overline{INT}$ and MSF when only MI enabled

Bit TI_TP is set to logic 1 resulting in $^{1}/_{64}$ Hz wide interrupt pulse.

Fig 9. $\overline{INT}$ example for bits SI and MI

Table 26. Effect of bits MI and SI on $\overline{INT}$ generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

The minute and second flag (bit MSF) is set to logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{INT}$ pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{INT}$ pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCA2125 and identify the source of the interrupt such as the minute/second or countdown timer.

Table 27. Effect of bits MI and SI on bit MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments[1]
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

[1] In the case of bit MI = 1 and bit SI = 0, bit MSF will be cleared automatically after 1 second.

8.6.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4096 Hz, 64 Hz, 1 Hz, or $1/60$ Hz), and enables or disables the timer.

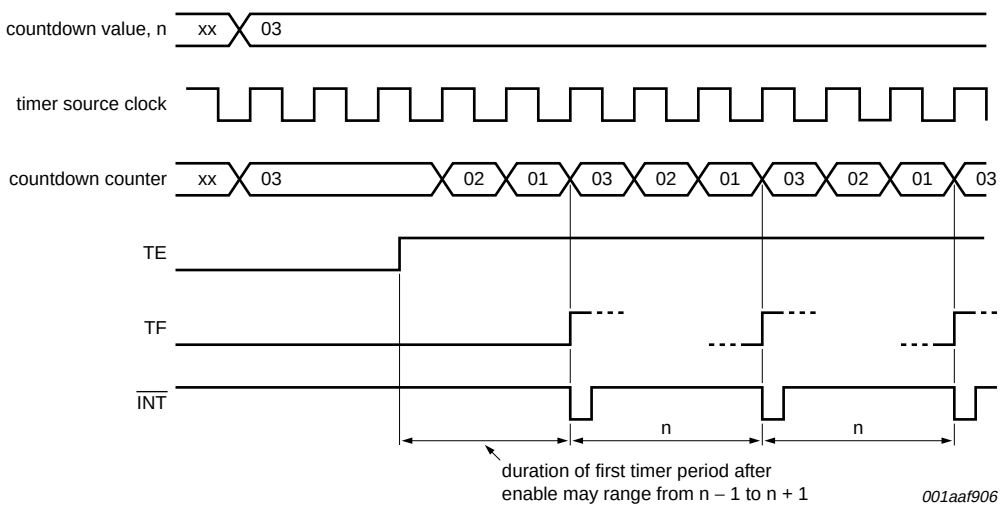
Table 28. Bits CTD1 and CTD0 for timer frequency selection and countdown timer durations

Bits CTD[1:0]	Timer source clock frequency	Delay	
		Minimum timer duration n = 1	Maximum timer duration n = 255
00	4096 Hz	244 µs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz	1 s	255 s
11	$1/60$ Hz	60 s[1]	4 h 15 min

[1] When not in use, bits CTD[1:0] must be set to $1/60$ Hz for power saving.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in a corresponding deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value n. Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter; see Figure 10.



In the example it is assumed that the timer flag is cleared before the next countdown period expires and that the $\overline{INT}$ is set to pulsed mode.

Fig 10. General countdown timer behavior

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP Semiconductors does not recommend changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous with the timer clock, therefore changing it without setting bit TE = 0 will result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value n will however be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 8.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous with the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock; see Table 29.

Table 29. First period delay for timer counter value n

Timer source clock	Minimum timer period	Maximum timer period
4096 Hz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF can only be cleared by software. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt can be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output can be disabled with bit TIE.

When reading the timer, the current countdown value is returned and **not** the initial value n. For accurate read back of the countdown value, the SPI-bus clock (SCL) must be operating at a frequency of at least twice the selected timer clock. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

8.6.3 Timer flags

When a minute or second interrupt occurs, bit MSF is set to logic 1. Similarly, at the end of a timer countdown, bit TF is set to logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. The flag is reset by writing a logic 0 but its value is not affected by writing a logic 1.

Three examples are given for clearing the flags. Flags MSF and TF are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 30. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 31, Table 32 and Table 33 show what instruction must be sent to clear the appropriate flag.

Table 31. Example to clear only TF (bit 2) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	1	0	-	-

Table 32. Example to clear only MSF (bit 5) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	1	-	-

Table 33. Example to clear both TF and MSF (bits 2 and 5) in register Control_2

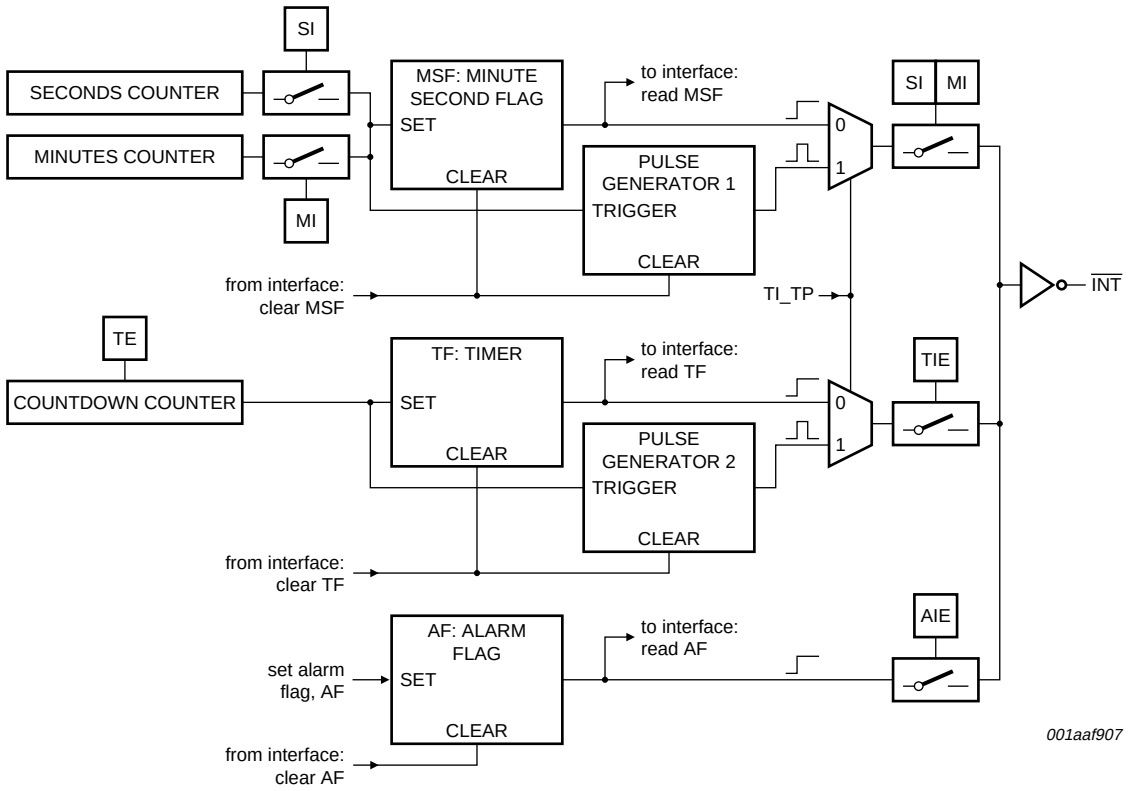
Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in exactly the same way; see Section 8.5.1.

8.7 Interrupt output

An active LOW interrupt signal is available at pin $\overline{\text{INT}}$. Operation is controlled via the bits of control register 2. Interrupts can be sourced from three places: second/minute timer, countdown timer and alarm function.

Bit TI_TP configures the timer generated interrupts to be either a pulse or to follow the status of the interrupt flags (bits TF and MSF).



When bits SI, MI, TIE and AIE are all disabled, pin $\overline{INT}$ will remain high-impedance.

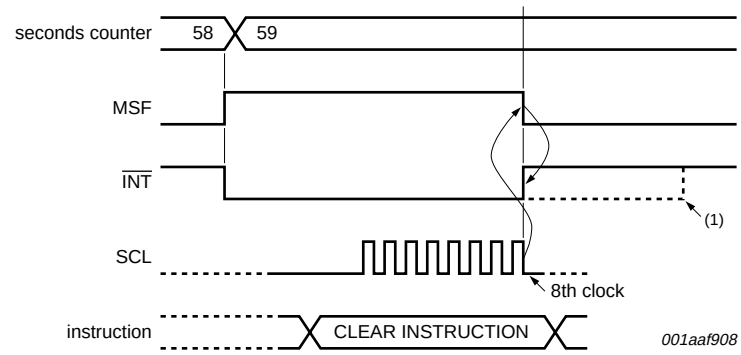
Fig 11. Interrupt scheme

Remark: Note that the interrupts from the three groups are wired-OR, meaning they will mask one another; see Figure 11.

8.7.1 Minute and second interrupts

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^{1}/_{64}$ second duration.

If the MSF flag is clear before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 12. Instructions for clearing MSF are given in Section 8.6.3.



(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 12. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag

The timing shown for clearing bit MSF in Figure 12 is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, where the pulse can be shortened by setting both bits MI and SI to logic 0.

8.7.2 Countdown timer interrupts

Generation of interrupts from the countdown timer is controlled via bit TIE; see Table 7.

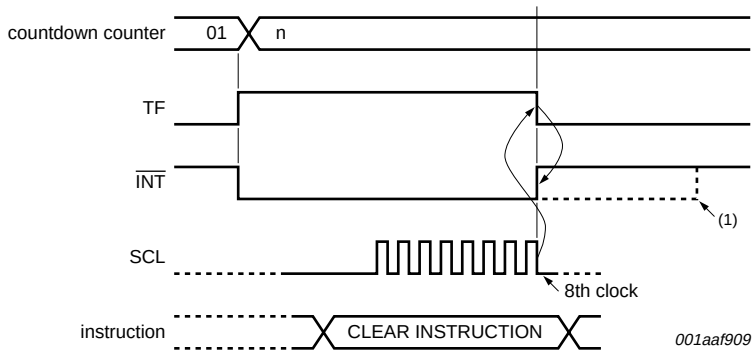
The pulse generator for the countdown timer interrupt also uses an internal clock which is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies; see Table 34.

Table 34. $\overline{INT}$ operation (bit TI_TP = 1)

Source clock (Hz)	$\overline{INT}$ period (s)	
	n = 1[1]	n > 1
4096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is clear before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced i.e. the system does not have to wait for the completion of the pulse before continuing; see Figure 13. Instructions for clearing TF are given in Section 8.6.3.



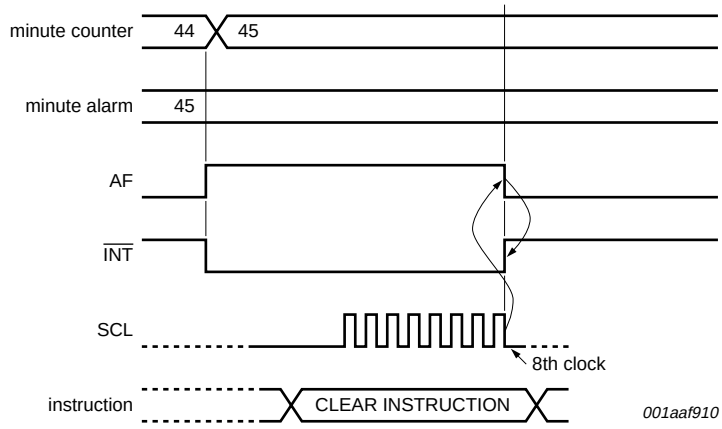
(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 13. Example of shortening the $\overline{INT}$ pulse by clearing the TF flag

The timing shown for clearing bit TF in Figure 13 is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, where the pulse can be shortened by setting bit TIE = 0.

8.7.3 Alarm interrupts

Generation of interrupts from the alarm function is controlled via bit AIE. If bit AIE is enabled, the $\overline{INT}$ pin follows the status of bit AF. Clearing bit AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts; see Figure 14.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 14. AF timing

8.8 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by control bits COF[2:0] in register CLKOUT_control (0Dh). Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is LOW.

The duty cycle of the selected clock is not controlled, but due to the nature of the clock generation, all clock frequencies, except 32.768 kHz, have a duty cycle of 50 : 50.

The 'stop' function can also affect the CLKOUT signal, depending on the selected frequency. When 'stop' is active, the CLKOUT pin will generate a continuous LOW for those frequencies that can be stopped. For more details, see Section 8.10.

Table 35. CLKOUT frequency selection

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1] (%)	Effect of 'stop'
000	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1	50 : 50	CLKOUT = LOW
111	CLKOUT = LOW		

[1] Duty cycle definition: HIGH-level time (%) : LOW-level time (%).

8.9 External clock test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1 making pin CLKOUT an input. The test mode replaces the internal signal with the signal applied to pin CLKOUT. Every 64 positive edges applied to pin CLKOUT generates an increment of one second.

The signal applied to pin CLKOUT should have a minimum HIGH width of 300 ns and a minimum period of 1000 ns. The internal clock, now sourced from pin CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler; see Section 8.10. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. STOP must be cleared before the prescaler can operate again.

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

8.10 STOP bit function

The STOP bit function allows the accurate starting of the time circuits. The stop function will cause the upper part of the prescaler (F_2 to F_{14}) to be held at reset, thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the stop is released; see Figure 15.

Stop will not affect the output of 32768 Hz, 16384 Hz or 8192 Hz; see Section 8.8.

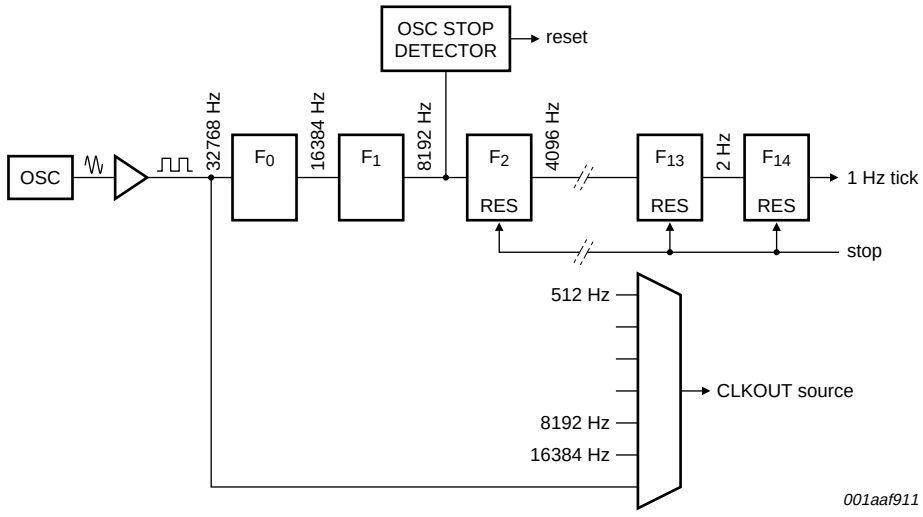


Fig 15. Stop bit functional diagram

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8192 Hz cycle; see Figure 16.

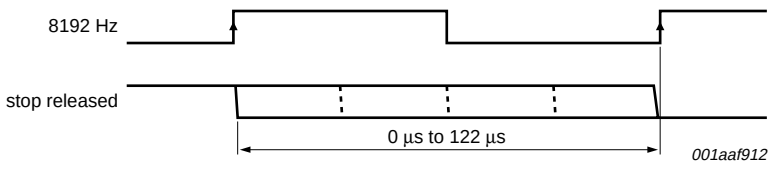


Fig 16. STOP bit release timing

The first increment of the time circuits is between 0.499888 s and 0.500000 s after stop is released. The uncertainty is caused by prescaler bits F0 and F1 not being reset; see Table 36.

Table 36. Example: first increment of time circuits after stop release

Bit STOP	Prescaler bits F_0F_1-F_2 to F_{14}[1]	1 Hz tick	Time hh:mm:ss	Comment
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
Stop is activated by user. F0F1 are not reset and values can not be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
Stop is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	
	XX-0 1000 0000 0000		08:00:00	
	XX-1 1000 0000 0000		08:00:00	
	:		:	
	11-1 1111 1111 1110		08:00:00	
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F14 increments the time circuits
	10-0 0000 0000 0001		08:00:01	
	:		:	
	11-1 1111 1111 1111		08:00:01	
	00-0 0000 0000 0000		08:00:01	
	10-0 0000 0000 0000		08:00:01	
	:		:	
	11-1 1111 1111 1110		08:00:01	
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F14 increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

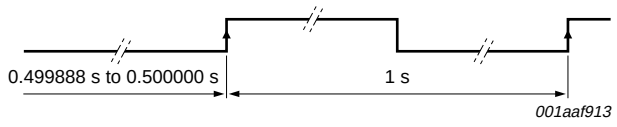


Fig 17. Increment of time circuit

8.11 3-line SPI

Data transfer to and from the device is made via a 3-wire SPI-bus; see Table 37. The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first; see Figure 18.

Table 37. Serial interface

Pin	Function	Description
CE	chip enable input	when LOW, the interface is reset; pull-down resistor included; active input can be higher than V_{DD}, but must not be wired HIGH permanently
SCL	serial clock input	when pin CE = LOW, this input might float; input can be higher than V_{DD}
SDI	serial data input	when pin CE = LOW, this input might float; input can be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from V_{SS} to V_{DD}; output data is changed on the falling edge of SCL

The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Data is captured on the rising edge of the clock and transferred internally on the falling edge.

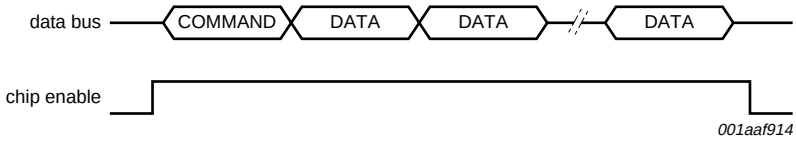


Fig 18. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The read/write bit (R/$\overline{W}$) defines if the following bytes will be read or write information.

Table 38. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or data write selection
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes will cause the device to ignore data transfer
3 to 0	RA	00h to 0Fh	register address range

In Figure 19 the Seconds register is set to 45 seconds and the Minutes register to 10 minutes.

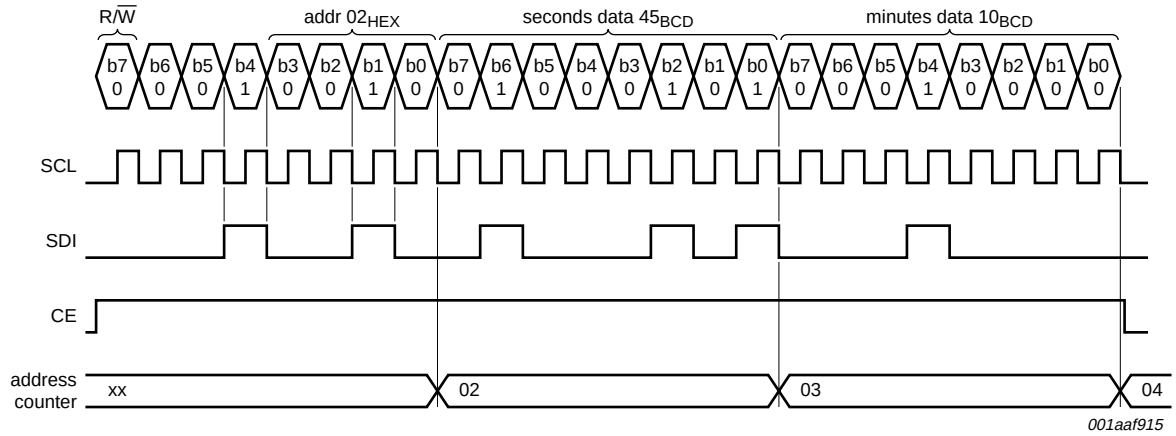


Fig 19. Serial bus write example

In Figure 20 the Months and Years registers are read. In this example, pins SDI and SDO are not connected together. In this configuration, it is important that pin SDI is never left floating: it must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents will result.

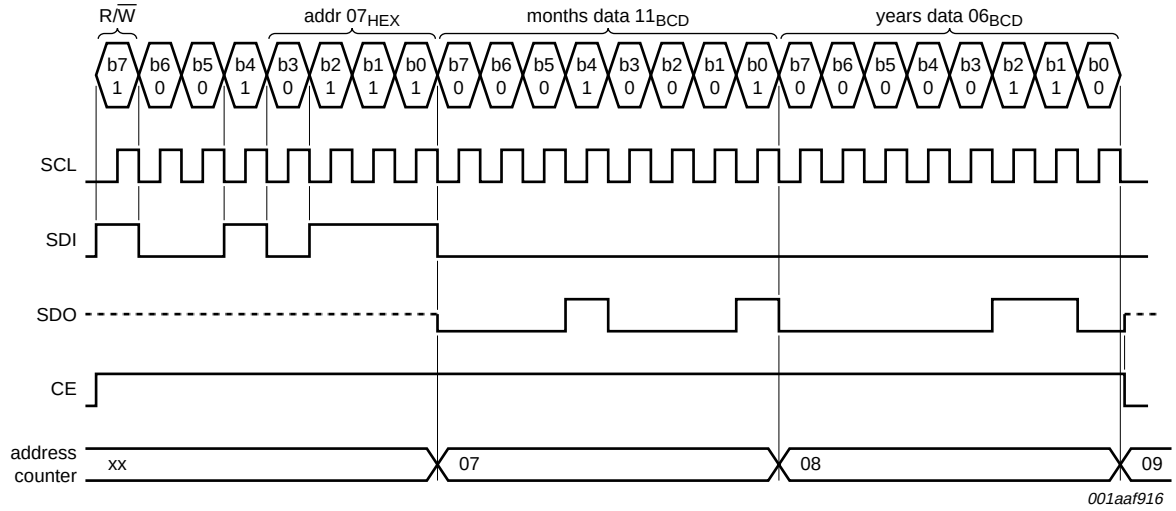


Fig 20. Serial bus read example

9. Internal circuitry

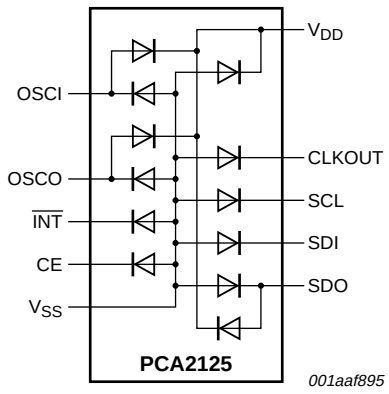


Fig 21. Device diode protection diagram

10. Limiting values

Table 39. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+6.5	V
I_{DD}	supply current			–50	+50	mA
V_I	input voltage			–0.5	+6.5	V
V_O	output voltage			–0.5	+6.5	V
I_I	input current			–10	+10	mA
I_O	output current			–10	+10	mA
P_{tot}	total power dissipation			-	300	mW
T_{amb}	ambient temperature			–40	+125	°C
T_{stg}	storage temperature			–65	+150	°C
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		MM	[2]	-	±200	V
		CDM	[3]	-	±2000	V
I_{lu}	latch-up current		[4]	-	100	mA

[1] HBM: Human Body Model, according to JESD22-A114.

[2] MM: Machine Model, according to JESD22-A115.

[3] CDM: Charged-Device Model, according to JESD22-C101.

[4] Latch-up testing, according to JESD78.

11. Static characteristics

Table 40. Static characteristics

V_{DD} = 1.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12.5 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply: pin V_{DD}							
V_{DD}	supply voltage	SPI-bus inactive; for clock data integrity	[1]	1.3	-	5.5	V
		SPI-bus active		1.6	-	5.5	V
I_{DD}	supply current	SPI-bus active					
		f_{SCL} = 6.0 MHz		-	-	500	µA
		f_{SCL} = 1.0 MHz		-	-	85	µA
		SPI-bus inactive; CLKOUT disabled; V_{DD} = 2.0 V to 5.0 V	[2]				
		T_{amb} = 25 °C		-	550	-	nA
		T_{amb} = −40 °C to +125 °C		-	760	1800	nA
		SPI-bus inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz					
		T_{amb} = 25 °C					
		V_{DD} = 5.0 V		-	1000	-	nA
		V_{DD} = 3.0 V		-	760	-	nA
		V_{DD} = 2.0 V		-	640	-	nA
		T_{amb} = −40 °C to +125 °C					
		V_{DD} = 5.0 V		-	-	2250	nA
		V_{DD} = 3.0 V		-	-	1950	nA
		V_{DD} = 2.0 V		-	-	1900	nA
Inputs							
V_I	input voltage	pin OSCI		−0.5	-	V_{DD} + 0.5	V
V_I	input voltage	pins CE, SDI, SCL		−0.5	-	5.5	V
V_{IL}	LOW-level input voltage			V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	V_{DD}	V
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins SDI, SCL and OSCI		−1	0	+1	µA
C_I	input capacitance		[3]	-	-	7	pF
R_{pd}	pull-down resistance	pin CE		-	240	550	kΩ
Outputs							
V_O	output voltage	pins OSCO and SDO		-	-	V_{DD} + 0.5	V
V_O	output voltage	pins CLKOUT and $\overline{INT}$; refers to external pull-up voltage		-	-	5.5	V
V_{OH}	HIGH-level output voltage	pin SDO		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	pin SDO		V_{SS}	-	$0.2V_{DD}$	V
V_{OL}	LOW-level output voltage	pins CLKOUT and $\overline{INT}$; V_{DD} = 5 V; I_{OL} = 1.5 mA		V_{SS}	-	0.4	V

Table 40. Static characteristics *...continued*

V_{DD} = 1.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12.5 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OH}	HIGH-level output current	pin SDO; V_{OH} = 4.6 V; V_{DD} = 5 V	-	-	1.5	mA
I_{OL}	LOW-level output current	pins $\overline{INT}$, SDO and CLKOUT; V_{OL} = 0.4 V; V_{DD} = 5 V	−1.5	-	-	mA
I_{OL}	LOW-level output current	pin OSCO; V_{OL} = 0.4 V; V_{DD} = 5 V	−1	-	-	mA
I_{LO}	output leakage current	V_O = V_{DD} or V_{SS}	−1	0	+1	µA
C_{ext}	external capacitance		-	25	-	pF

[1] For reliable oscillator start at power-up: V_{DD} = $V_{DD(min)}$ + 0.3 V.

[2] Timer source clock = $\frac{1}{60}$ Hz; voltage on pins CE, SDI and SCL at V_{DD} or V_{SS}.

[3] Implicit by design.

12. Dynamic characteristics

Table 41. Dynamic characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C.
All timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.6 V		V_{DD} = 2.7 V		V_{DD} = 4.5 V		V_{DD} = 5.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pin SCL											
$f_{clk(SCL)}$	SCL clock frequency		-	1.5	-	4.76	-	5.00	-	6.25	MHz
t_{SCL}	SCL time		660	-	210	-	200	-	160	-	ns
$t_{clk(H)}$	clock HIGH time		320	-	100	-	100	-	70	-	ns
$t_{clk(L)}$	clock LOW time		320	-	110	-	100	-	90	-	ns
t_r	rise time		-	100	-	100	-	100	-	100	ns
t_f	fall time		-	100	-	100	-	100	-	100	ns
Pin CE											
$t_{su(CE)}$	CE set-up time		30	-	30	-	30	-	30	-	ns
$t_{h(CE)}$	CE hold time		100	-	60	-	40	-	30	-	ns
$t_{rec(CE)}$	CE recovery time		100	-	100	-	100	-	100	-	ns
$t_{w(CE)}$	CE pulse width		-	0.99	-	0.99	-	0.99	-	0.99	s
Pin SDI											
t_{su}	set-up time		25	-	15	-	15	-	10	-	ns
t_h	hold time		100	-	60	-	40	-	30	-	ns
Pin SDO											
$t_{d(R)SDO}$	SDO read delay time	bus load = 85 pF	-	320	-	110	-	100	-	90	ns
$t_{dis(SDO)}$	SDO disable time	no load value [1]	-	50	-	30	-	30	-	25	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	0	-	0	-	ns

[1] Bus will be held up by bus capacitance; use RC time constant with application values.

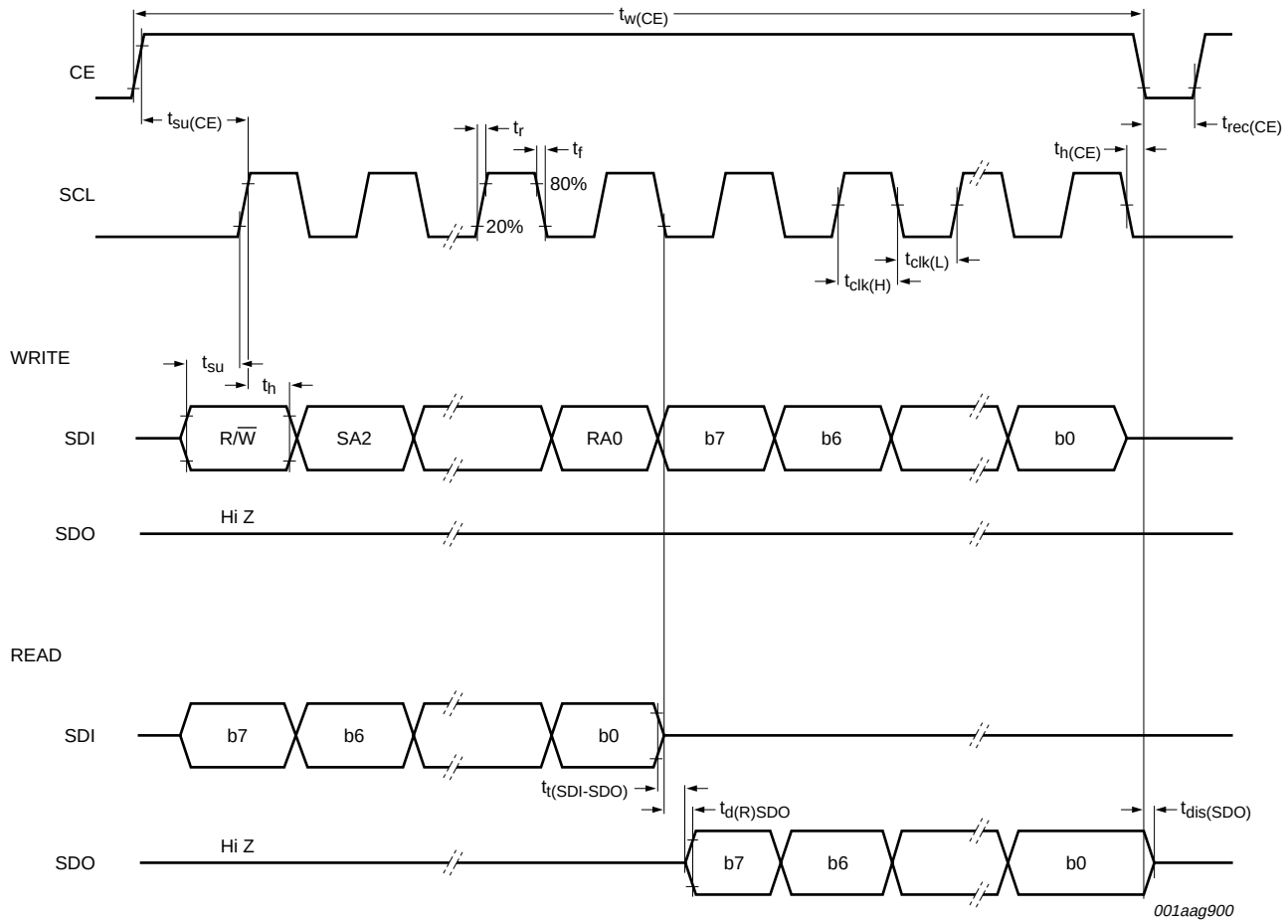
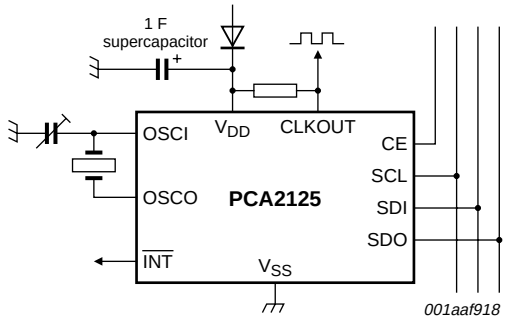


Fig 22. SPI interface timing

13. Application information

13.1 Application diagram



The 1 farad capacitor is used as a standby and back-up supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC can operate for several weeks.

Fig 23. Application diagram

13.2 Quartz frequency adjustment

1. Method 1: fixed OSCI capacitor

   A fixed capacitor can be used whose value can be determined by evaluating the average capacitance necessary for the application layout; see Figure 23. The frequency is best measured via the 32.768 kHz signal at pin CLKOUT available after power-on. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). An average deviation of ±5 minutes per year can be easily achieved.

2. Method 2: OSCI trimmer

   Fast setting of a trimmer is possible using the 32.768 kHz signal at pin CLKOUT available after power-on.

3. Method 3: OSCO output

   Direct measurement of OSCO output (accounting for test probe capacitance).

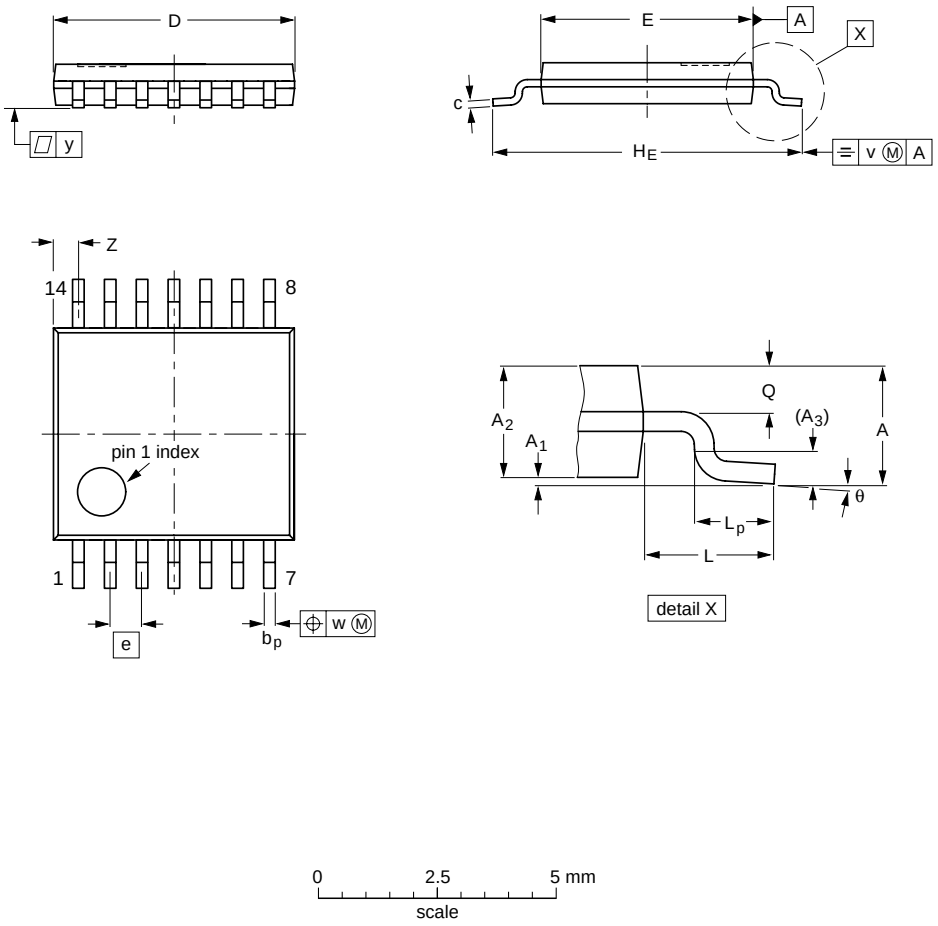
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 24. Package outline SOT402-1 (TSSOP14)

16. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling MOS devices; see *JESD625-A and/or IEC61340-5*.

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 42 and 43

Table 42. SnPb eutectic process (from J-STD-020C)

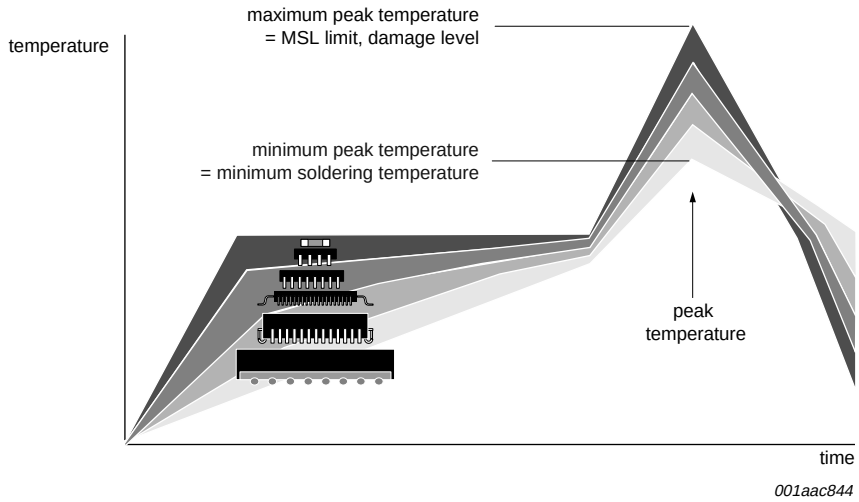
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 43. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Revision history

Table 44. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA2125_1	20080728	Product data sheet		-

19. Legal information

20. Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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