

# MC74HCT20A

## Dual 4-Input NAND Gate with LSTTL-Compatible Inputs

### High-Performance Silicon-Gate CMOS

The MC74HCT20A is identical in pinout to the LS20. The device inputs are compatible with standard CMOS LSTTL outputs.

#### Features

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 V to 5.5 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb-Free Devices

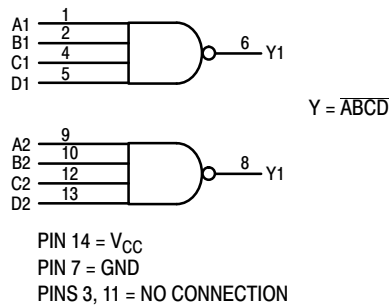


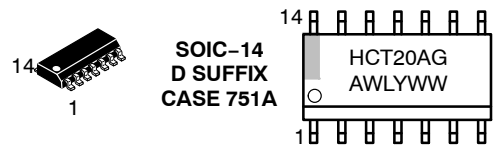
Figure 1. Logic Diagram



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#### MARKING DIAGRAMS



A = Assembly Location  
 WL, L = Wafer Lot  
 YY, Y = Year  
 WW, W = Work Week  
 G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN ASSIGNMENT

A1	1	14	$V_{CC}$
B1	2	13	D2
NC	3	12	C2
C1	4	11	NC
D1	5	10	B2
Y1	6	9	A2
GND	7	8	Y2

#### FUNCTION TABLE

Inputs				Output
A	B	C	D	Y
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H
H	H	H	H	L

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC74HCT20A

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit	
$V_{CC}$	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V	
$V_{in}$	DC Input Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V	
$V_{out}$	DC Output Voltage (Referenced to GND)	-0.5 to $V_{CC} + 0.5$	V	
$I_{in}$	DC Input Current, per Pin	$\pm 20$	mA	
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA	
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA	
$P_D$	Power Dissipation in Still Air	SOIC Package TSSOP Package	500 450	mW
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
$V_{in}, V_{out}$	DC Input Voltage, Output Voltage (Referenced to GND)	0	$V_{CC}$	V
$T_A$	Operating Temperature Range, All Package Types	-55	+125	$^{\circ}C$
$t_r, t_f$	Input Rise/Fall Time (Figure 1)	0	500	ns

## DC CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Condition	$V_{CC}$ V	Guaranteed Limit			Unit
				-55 to 25 $^{\circ}C$	$\leq 85^{\circ}C$	$\leq 125^{\circ}C$	
$V_{IH}$	Minimum High-Level Input Voltage	$V_{out} = 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	2.0	2.0	2.0	V
			5.5	2.0	2.0	2.0	
$V_{IL}$	Maximum Low-Level Input Voltage	$V_{out} = V_{CC} - 0.1V$ $ I_{out}  \leq 20\mu A$	4.5	0.8	0.8	0.8	V
			5.5	0.8	0.8	0.8	
$V_{OH}$	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out}  \leq 20\mu A$	4.5	4.4	4.4	4.4	V
			5.5	5.4	5.4	5.4	
$V_{OL}$	Maximum Low-Level Output Voltage	$V_{in} = V_{IH}$ $ I_{out}  \leq 20\mu A$	4.5	0.1	0.1	0.1	V
			5.5	0.1	0.1	0.1	
$I_{in}$	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	4.5	0.26	0.33	0.40	$\mu A$
			5.5	$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	
$I_{CC}$	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0\mu A$	4.5	1	10	40	$\mu A$
			5.5				
$\Delta I_{CC}$	Additional Quiescent Supply Current	$V_{in} = 2.4V$ , Any One Input $V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\mu A$	5.5	$\geq -55^{\circ}C$	25 to 125 $^{\circ}C$		mA
					2.9	2.4	

- Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).
- Total Supply Current =  $I_{CC} + \Sigma \Delta I_{CC}$ .

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## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50 \text{ pF}$ , Input $t_r = t_f = 6 \text{ ns}$ , $V_{CC} = 5.0 \text{ V}$ )

Symbol	Parameter	Guaranteed Limit			Unit
		- 55 to 25°C	≤ 85°C	≤ 125°C	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, Input A, B, or C to Output Y (Figures 2 and 3)	28	35	42	ns
$t_{TLH}$ , $t_{THL}$	Maximum Output Transition Time, Any Output (Figures 2 and 3)	15	19	22	ns
$C_{in}$	Maximum Input Capacitance	10	10	10	pF

$C_{PD}$	Power Dissipation Capacitance (Per Gate)	Typical @ 25°C, $V_{CC} = 5.0 \text{ V}$		pF
		26		

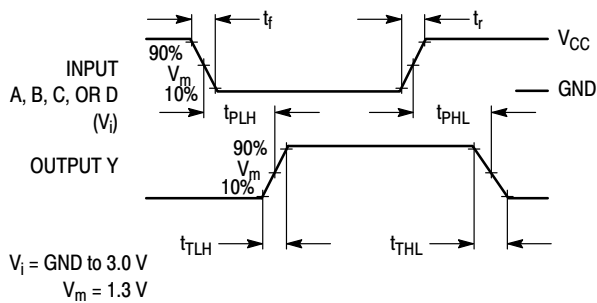
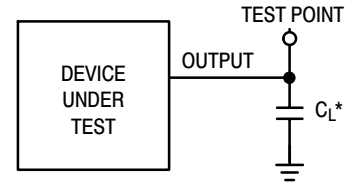


Figure 2. Switching Waveforms



\*Includes all probe and jig capacitance

Figure 3. Test Circuit

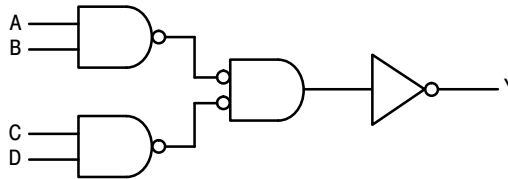


Figure 4. Expanded Logic Diagram  
(1/2 of the Device)

## ORDERING INFORMATION

Device	Package	Shipping†
MC74HCT20ADG	SOIC-14 (Pb-Free)	55 Units/Rail
MC74HCT20ADR2G	SOIC-14 (Pb-Free)	2500/Tape & Reel
MC74HCT20ADTR2G	TSSOP-14*	

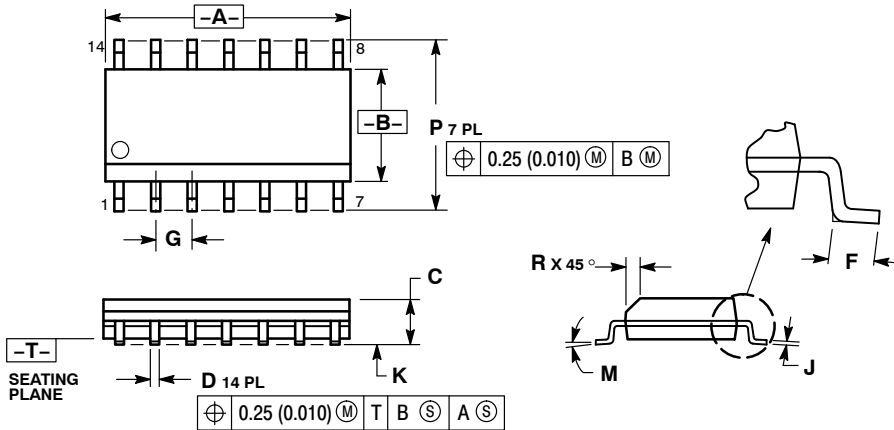
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## PACKAGE DIMENSIONS

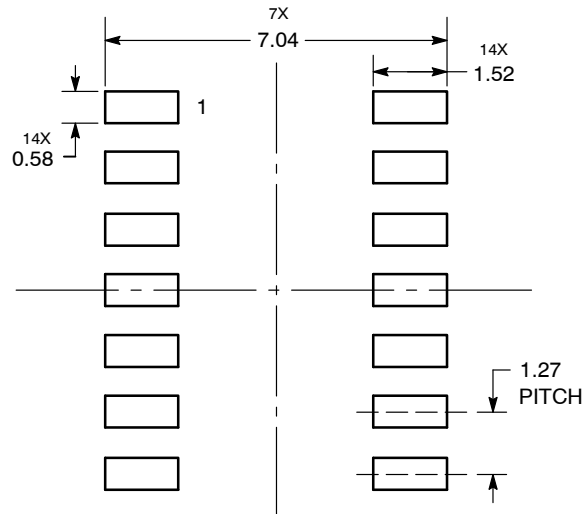
SOIC-14  
CASE 751A-03  
ISSUE J



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

### SOLDERING FOOTPRINT\*



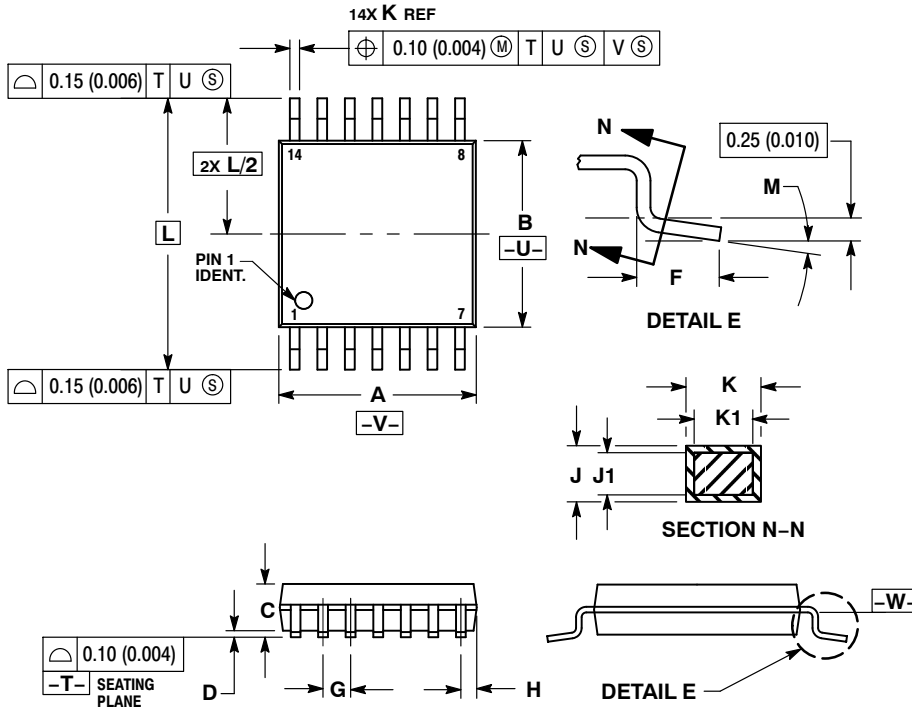
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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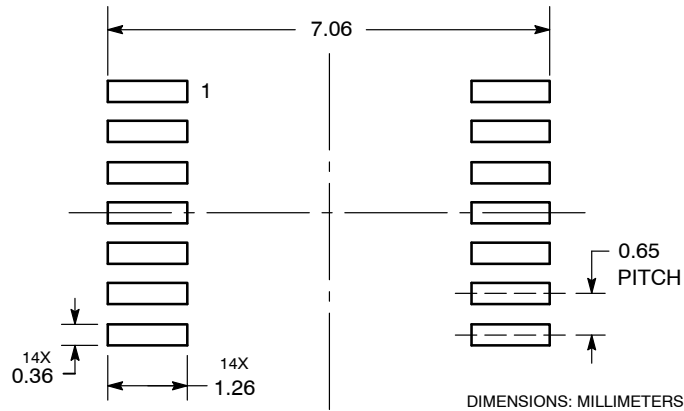
## PACKAGE DIMENSIONS

TSSOP-14  
CASE 948G-01  
ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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