

EMD5DXV6T1, EMD5DXV6T5

Preferred Devices

Product Preview Dual Bias Resistor Transistors

NPN and PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

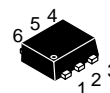
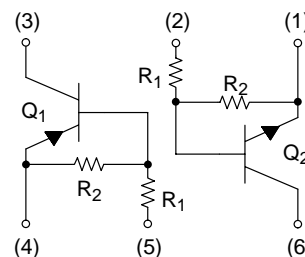
The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the EMD5DXV6T1 series, two complementary BRT devices are housed in the SOT-563 package which is ideal for low power surface mount applications where board space is at a premium.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Available in 8 mm, 7 inch Tape and Reel
- Lead Free Solder Plating



ON Semiconductor®

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SOT-563
CASE 463A
PLASTIC

MARKING DIAGRAM



U5 = Specific Device Code
D = Date Code

ORDERING INFORMATION

Device	Package	Shipping
EMD5DXV6T1	SOT-563	4 mm pitch 4000/Tape & Reel
EMD5DXV6T5	SOT-563	2 mm pitch 8000/Tape & Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

Preferred devices are recommended choices for future use and best overall value.

EMD5DXV6T1, EMD5DXV6T5

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted, common for Q₁ and Q₂, – minus sign for Q₁ (PNP) omitted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CB0}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mA _{dc}

THERMAL CHARACTERISTICS

Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation Derate above 25°C	P_D	357 (Note 1) 2.9 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	°C/W
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation Derate above 25°C	P_D	500 (Note 1) 4.0 (Note 1)	mW mW/°C
Thermal Resistance Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	°C/W
Junction and Storage Temperature	T_J, T_{stg}	-55 to +150	°C

1. FR-4 @ Minimum Pad

EMD5DXV6T1, EMD5DXV6T5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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Q1 TRANSISTOR: PNP

OFF CHARACTERISTICS

Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0, I _C = 5.0 mA)	I _{EBO}	-	-	1.0	mAdc

ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	20	35	-	
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	-	-	Vdc
Input Resistor	R1	3.3	4.7	6.1	kΩ
Resistor Ratio	R1/R2	0.38	0.47	0.56	

Q2 TRANSISTOR: NPN

OFF CHARACTERISTICS

Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0)	I _{CBO}	-	-	100	nAdc
Collector-Emitter Cutoff Current (V _{CB} = 50 V, I _B = 0)	I _{CEO}	-	-	500	nAdc
Emitter-Base Cutoff Current (V _{EB} = 6.0, I _C = 5.0 mA)	I _{EBO}	-	-	0.1	mAdc

ON CHARACTERISTICS

Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0)	V _{(BR)CBO}	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (I _C = 2.0 mA, I _B = 0)	V _{(BR)CEO}	50	-	-	Vdc
DC Current Gain (V _{CE} = 10 V, I _C = 5.0 mA)	h _{FE}	80	140	-	
Collector-Emitter Saturation Voltage (I _C = 10 mA, I _B = 0.3 mA)	V _{CE(SAT)}	-	-	0.25	Vdc
Output Voltage (on) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ)	V _{OL}	-	-	0.2	Vdc
Output Voltage (off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ)	V _{OH}	4.9	-	-	Vdc
Input Resistor	R1	33	47	61	kΩ
Resistor Ratio	R1/R2	0.8	1.0	1.2	

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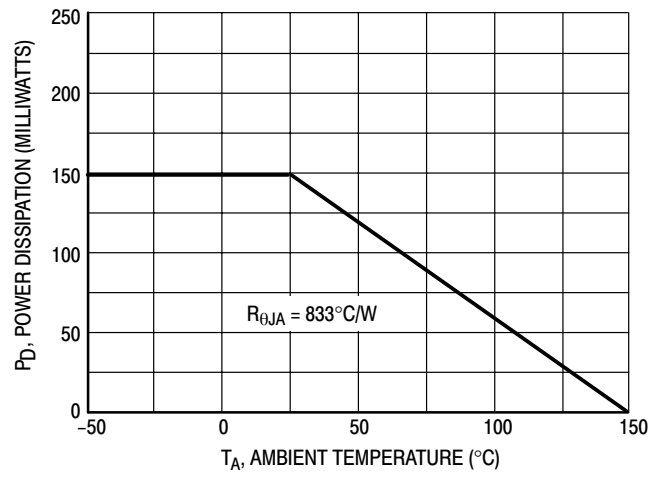


Figure 1. Derating Curve

EMD5DXV6T1, EMD5DXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS — EMD5DXV6T1 PNP TRANSISTOR

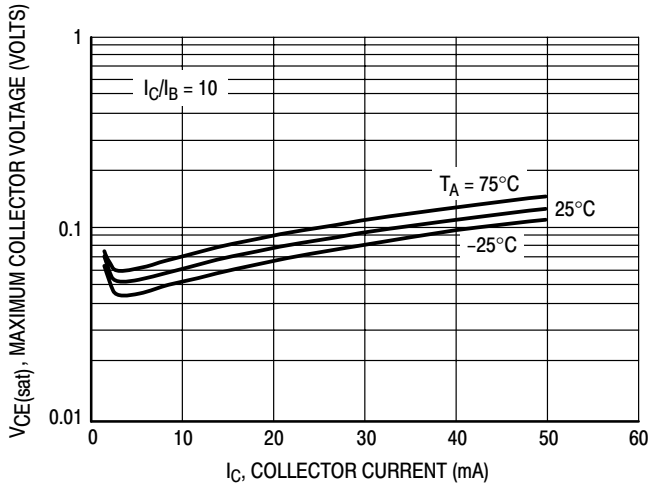


Figure 2. $V_{CE(sat)}$ versus I_C

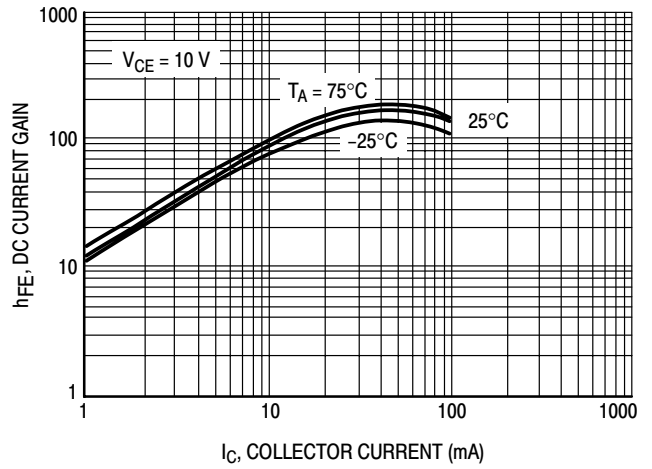


Figure 3. DC Current Gain

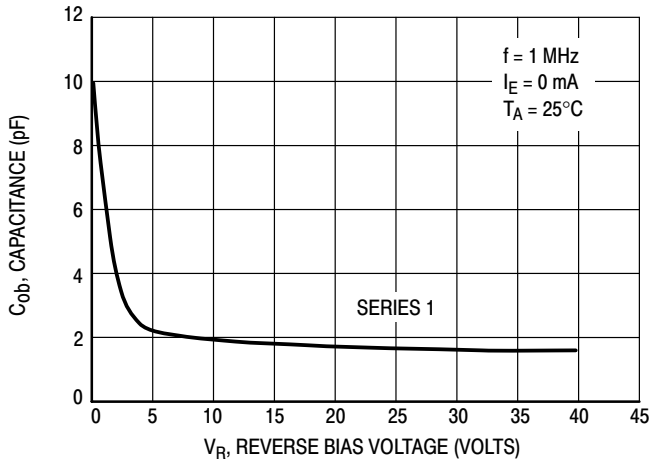


Figure 4. Output Capacitance

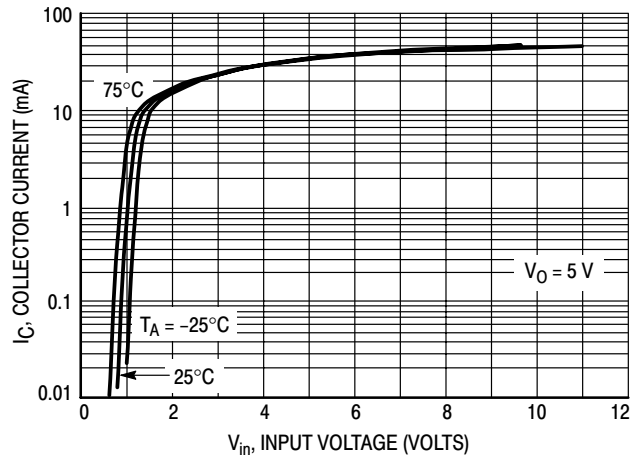


Figure 5. Output Current versus Input Voltage

EMD5DXV6T1, EMD5DXV6T5

TYPICAL ELECTRICAL CHARACTERISTICS — EMD5DXV6T1 NPN TRANSISTOR

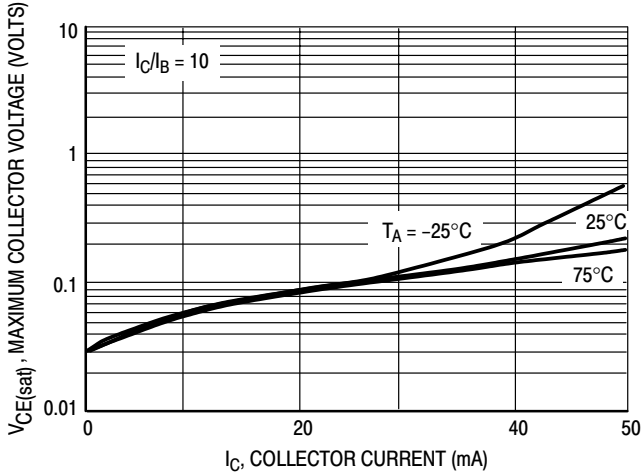


Figure 6. $V_{CE(sat)}$ versus I_C

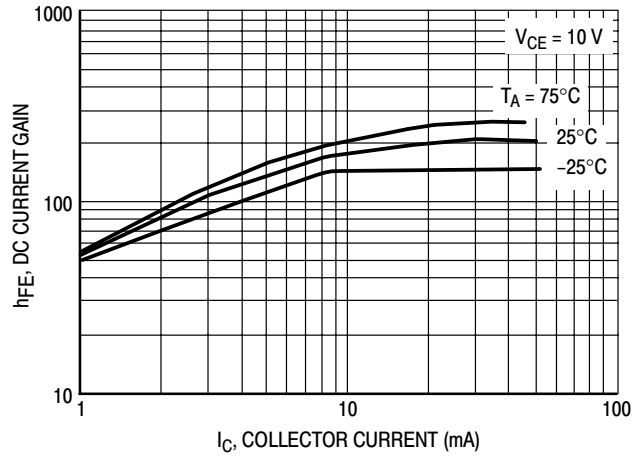


Figure 7. DC Current Gain

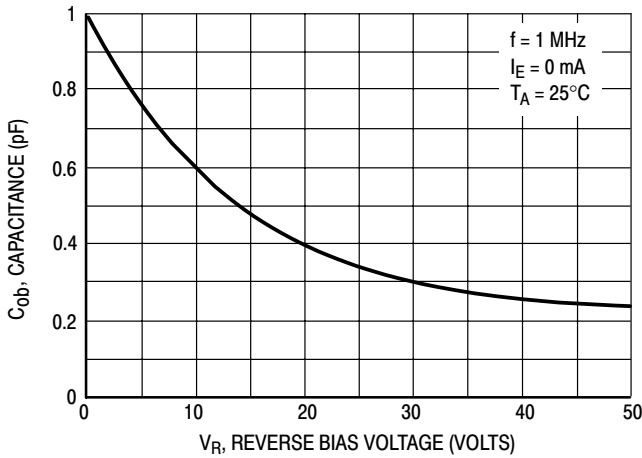


Figure 8. Output Capacitance

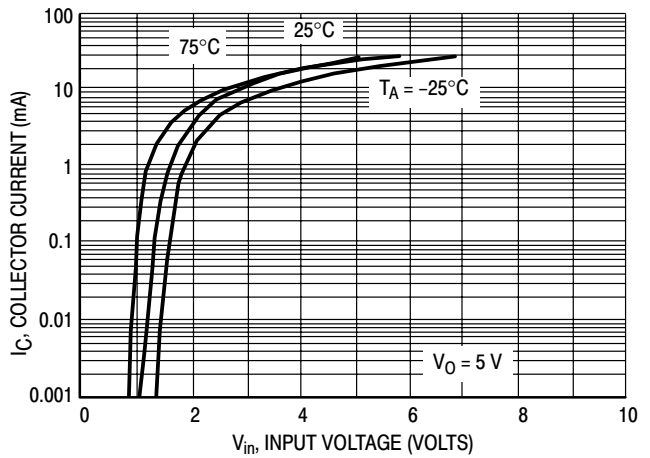


Figure 9. Output Current versus Input Voltage

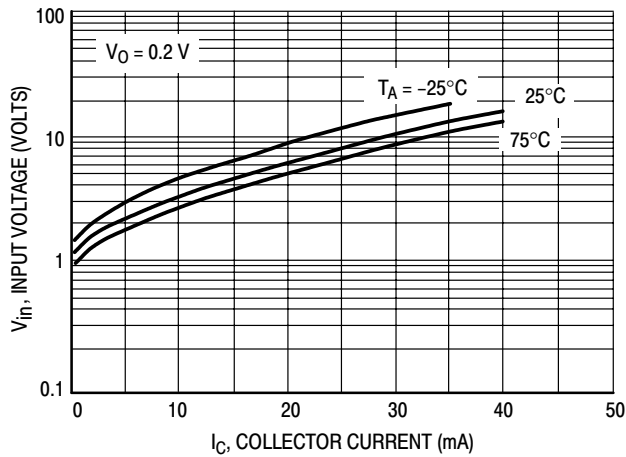


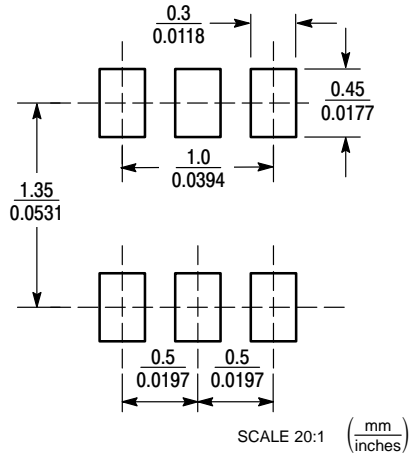
Figure 10. Input Voltage versus Output Current

INFORMATION FOR USING THE SOT-563 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



SOT-563

SOT-563 POWER DISSIPATION

The power dissipation of the SOT-563 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A . Using the values provided on the data sheet for the SOT-563 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{833^\circ\text{C/W}} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-563 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-563 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

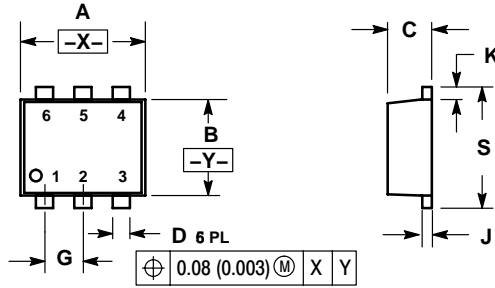
- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

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PACKAGE DIMENSIONS

SOT-563, 6 LEAD CASE 463A-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.50	1.70	0.059	0.067
B	1.10	1.30	0.043	0.051
C	0.50	0.60	0.020	0.024
D	0.17	0.27	0.007	0.011
G	0.50 BSC		0.020 BSC	
J	0.08	0.18	0.003	0.007
K	0.10	0.30	0.004	0.012
S	1.50	1.70	0.059	0.067

STYLE 1:

- PIN 1. EMITTER 1
- 2. BASE 1
- 3. COLLECTOR 2
- 4. EMITTER 2
- 5. BASE 2
- 6. COLLECTOR 1

STYLE 2:

- PIN 1. EMITTER 1
- 2. EMITTER2
- 3. BASE 2
- 4. COLLECTOR 2
- 5. BASE 1
- 6. COLLECTOR 1


STYLE 3:

- PIN 1. CATHODE 1
- 2. CATHODE 1
- 3. ANODE/ANODE 2
- 4. CATHODE 2
- 5. CATHODE 2
- 6. ANODE/ANODE 1

STYLE 4:

- PIN 1. COLLECTOR
- 2. COLLECTOR
- 3. BASE
- 4. EMITTER
- 5. COLLECTOR
- 6. COLLECTOR

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