AOZ1361DI

28V Programmable Current-Limited Load Switch

General Description

The AOZ1361DI is a high-side load switch intended for applications that require circuit protection. The device operates from voltages between 4.5V and 28V. The internal current limiting circuit protects the input supply voltage from large load current. The current limit can be set with an external resistor. The AOZ1361DI provides thermal protection function that limits excessive power dissipation. The device employs internal soft-start circuitry to control inrush current due to highly capacitive loads associated with hot-plug events. It features low quiescent current of 220µA and the supply current reduces to less than 1µA in shutdown.

The AOZ1361DI is available in a 10-pin 4x4 DFN package and can operate over -40°C to +85°C temperature range.

Features

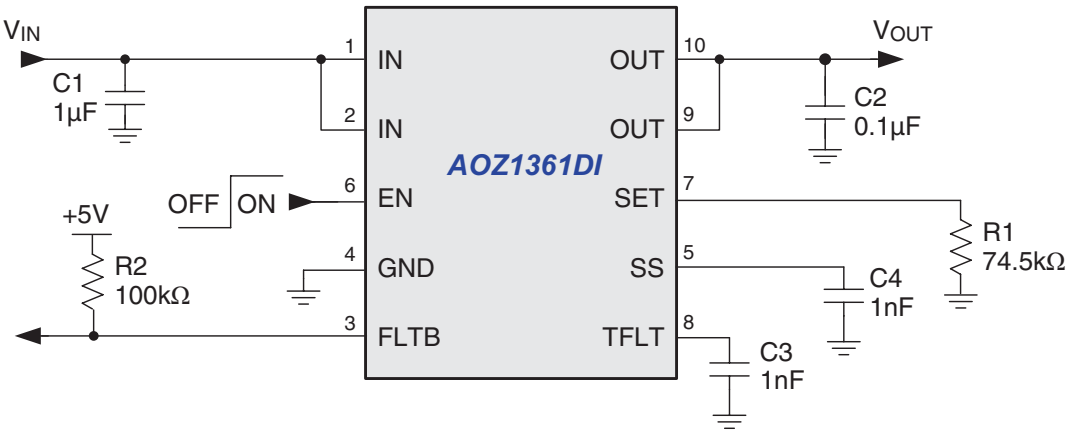
- 35mΩ maximum on resistance
- Programmable current limit
- 4.5V to 28V operating input voltage
- Low quiescent current
- Under-voltage lockout
- Thermal shutdown protection
- Open-drain fault indicator with delay
- Small 4x4 DFN package
- 2.5kV ESD rating

Applications

- Notebook PCs
- Hot swap supplies

Green Product

Typical Application



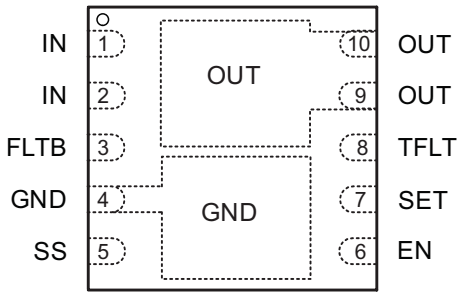
Ordering Information

Part Number	Feature	Package	Temperature Range	Environmental
AOZ1361DI-01	Auto-restart	DFN 4x4 10	-40°C to +85°C	RoHS Compliant Green Product
AOZ1361DI-02	Latch-off			

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

TOP VIEW



DFN 4x4 10

Pin Description

Pin Number	Pin Name	Pin Function
1, 2	IN	P-channel MOSFET source. Connect a 1µF capacitor from IN to GND.
3	FLTB	Fault output pin. This is an open drain output that is internally pulled low to indicate a fault condition. Connect to 5V or 3.3V through a pull up resistor.
4	GND	Ground.
5	SS	Soft-Start Pin. Connect a capacitor from SS to GND to set the soft-start time.
6	EN	Enable Input.
7	SET	Current Limit Set Pin. Connect a resistor between SET and GND to set the switch current limit.
8	TFLT	Fault Delay pin. Connect a capacitor from TFLT to GND to set the Fault delay time.
9, 10	OUT	P-channel MOSFET Drain. Connect a 0.1µF capacitor from OUT to GND.

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
IN to GND	-0.3V to +30V
EN, OUT to GND	-0.3V to V_{IN} + 0.3V
FLTB, TFLT, SS, SET	-0.3V to +6V
Maximum Junction Temperature (T_J)	+150°C
ESD Rating (HBM)	2.5kV

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Maximum Recommended Operating Conditions.

Parameter	Rating
Thermal Resistance (DFN 4x4)	63°C/W

Electrical Characteristics

V_{IN} = 12V, T_A = 25°C unless otherwise stated.

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
V_{IN}	Input Supply Voltage		4.5		28	V
V_{UVLO}	Undervoltage Lockout Threshold	IN rising		3.9	4.4	V
V_{UVHYS}	Undervoltage Lockout Hysteresis			200		mV
I_{IN_ON}	Input Quiescent Current	EN = IN, no load		300	500	µA
I_{IN_OFF}	Input Shutdown Current	EN = GND, no load			1	µA
I_{LEAK}	Output Leakage Current	EN = GND, no load			1	µA
$R_{DS(ON)}$	Switch On Resistance	V_{IN}= 12V		22	35	mΩ
		V_{IN} = 4.5V		33	43	
I_{LIM}	Current Limit	R_{SET} = 74.5kΩ	2	2.7	3.4	A
V_{EN_L}	Enable Input Low Voltage				0.8	V
V_{EN_H}	Enable Input High Voltage		2.0			V
V_{EN_HYS}	Enable Input Hysteresis			100		mV
I_{EN_BIAS}	Enable Input Bias Current				1	µA
Td_on	Turn-On Delay Time EN_50% to OUT_10%	R_L=120Ω, C_L = 1µF, SS = Floated. Measure from 50% of EN voltage to 10% of OUT voltage		280		µs
t_{ON}	Turn-On Rise Time OUT_10% to 90%	R_L=120Ω, C_L = 1µF, SS = Floated. Measure from 10% of OUT voltage to 90% of OUT voltage		220		µs
		R_L=120Ω, C_L = 1µF, C_{SS} = 1nF		360		µs
t_{OFF}	Turn-Off Fall Time	R_L=120Ω, C_L = 1µF, SS = Floated		280		µs
$R_{DS(FLTB)}$	On-Resistance at FLTB	Sink current = 4mA			100	Ω
I_{LEAK_FLT}	FLT Output Leakage				1	µA
TFLT	FLT Delay Period	C_{TLT} = 1nF		600		µs
T_{SD}	Thermal Shutdown Threshold			130		°C
T_{SD_HYS}	Thermal Shutdown Hysteresis			30		°C

Timing Diagram

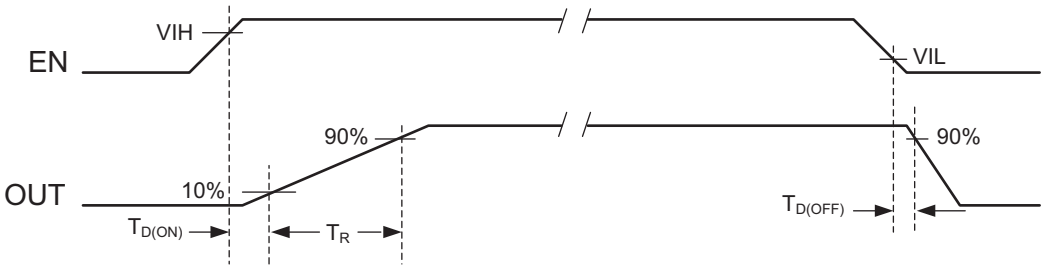


Figure 1. AOZ1361DI Timing

Functional Block Diagram

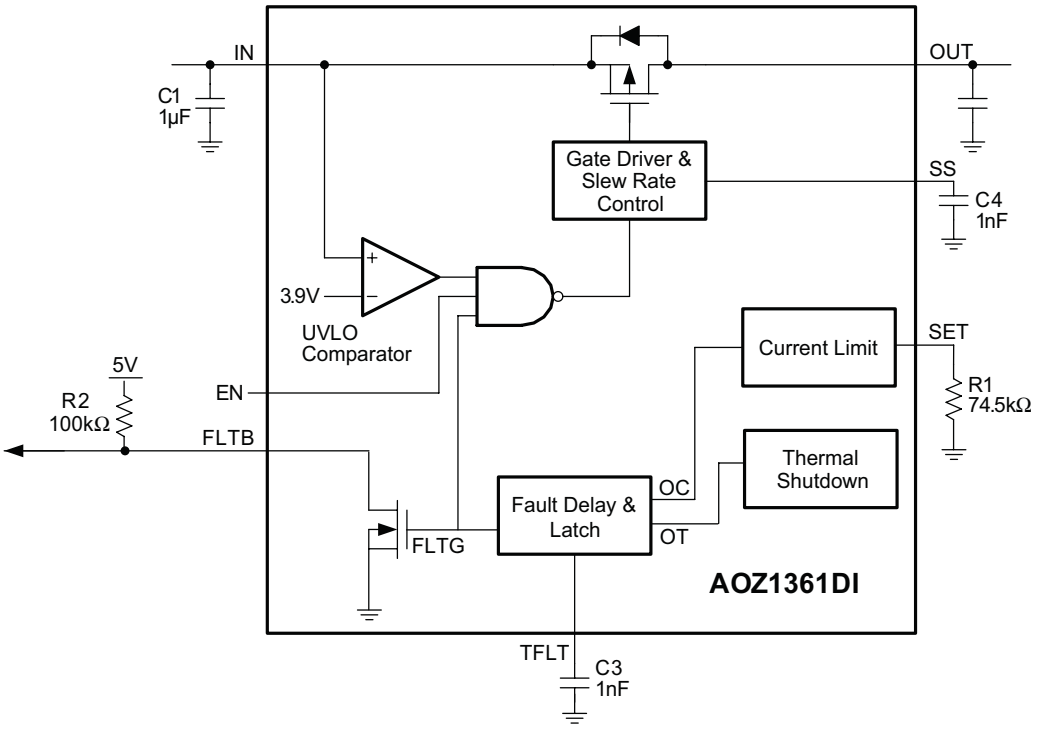
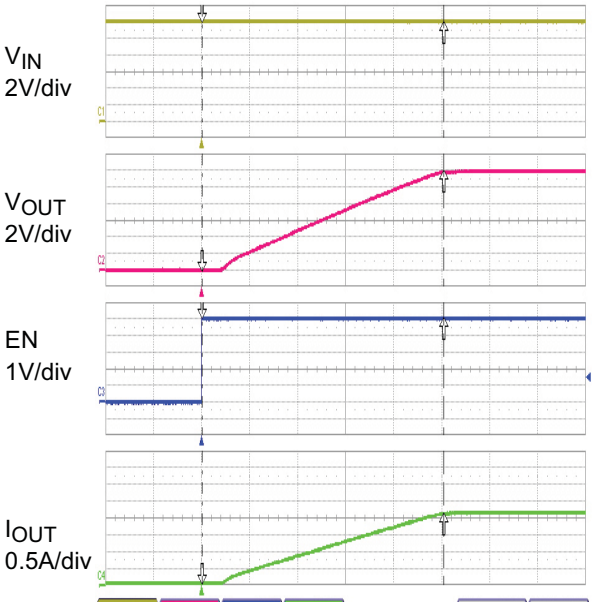


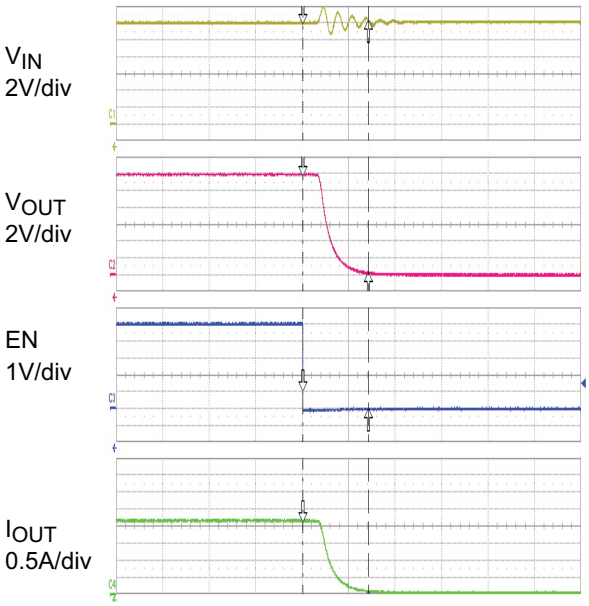
Figure 2. AOZ1361DI Functional Block Diagram

Functional Characteristics

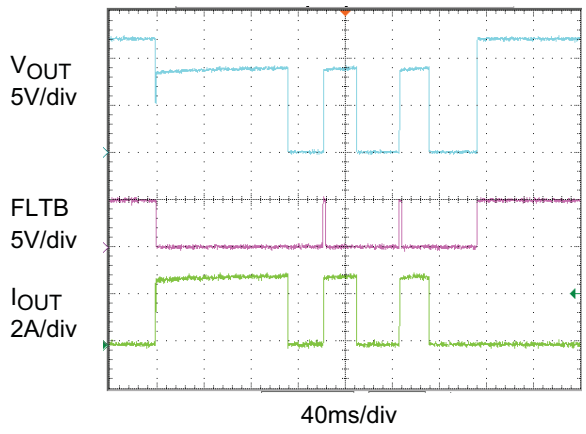
Turn-On
(V_{IN} = 12V, R_L = 5.6Ω, C4 = 0.01uF)



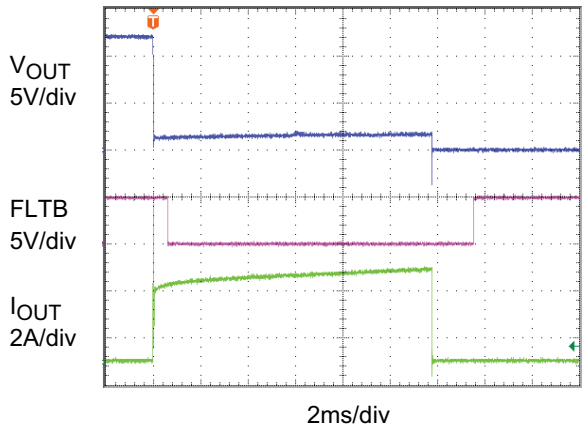
Turn-Off
(V_{IN} = 12V, R_L = 5.6Ω, C4 = 0.01uF)



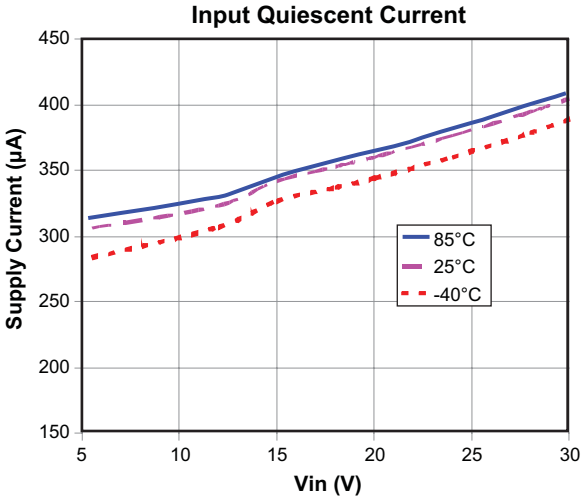
Current Limit Response Thermal Shutdown
AOZ1361DI-01: Auto-Restart Version
(V_{IN} = 12V)

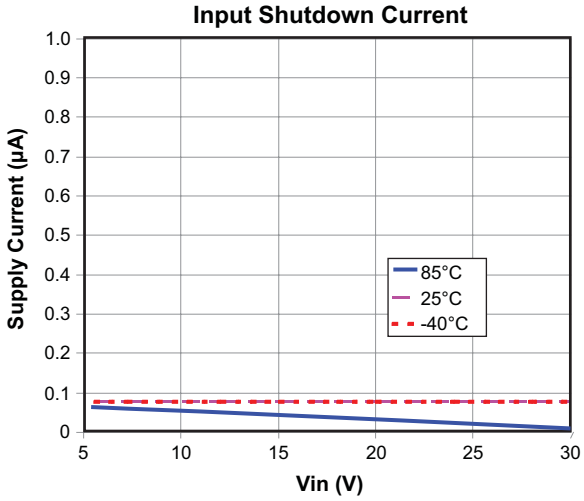


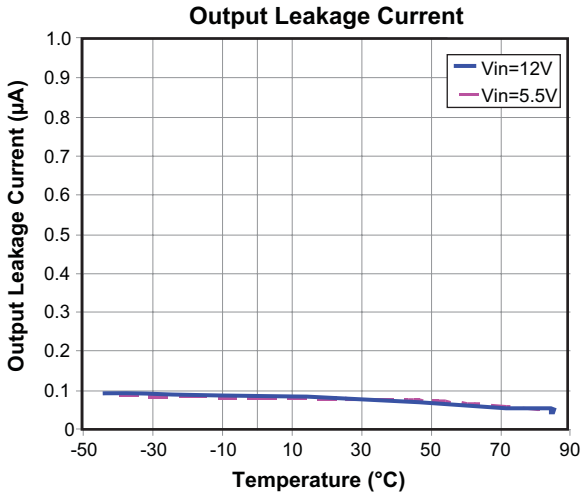
Current Limit Response Thermal Shutdown
AOZ1361DI-02: Latch-off Version
(V_{IN} = 12V)

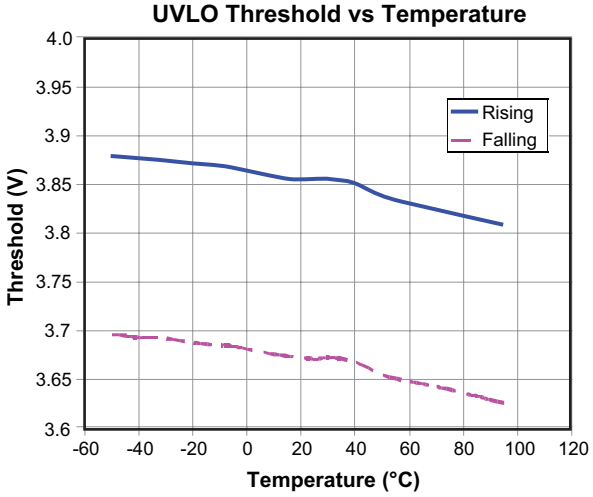


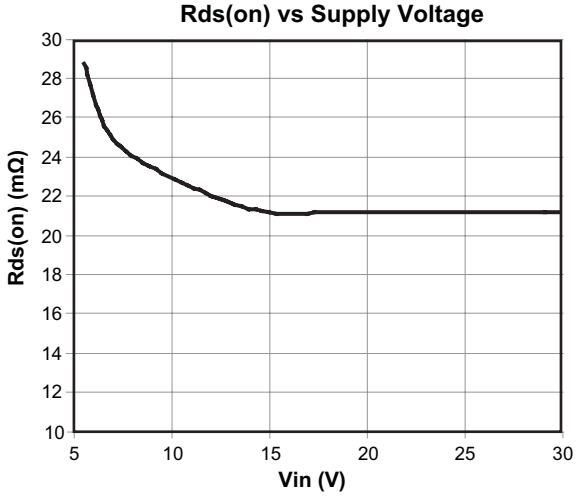
Typical Operating Characteristics

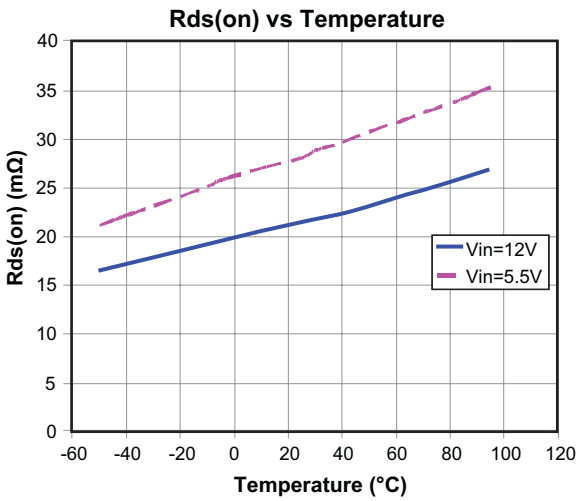






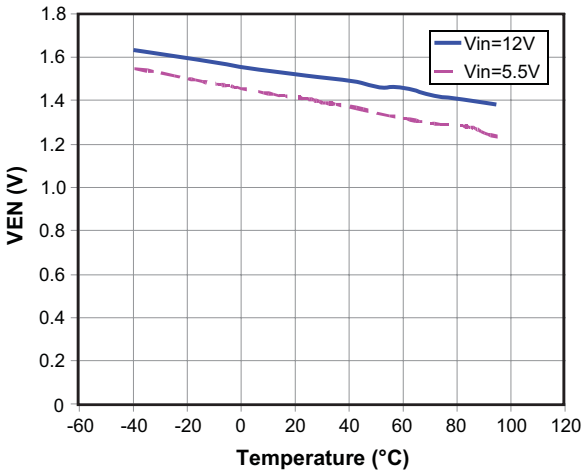




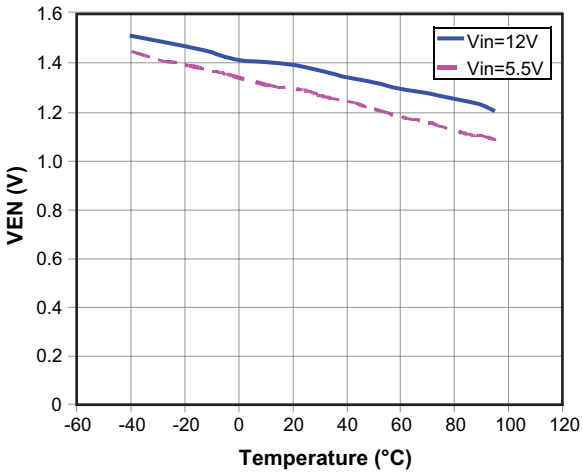


Typical Operating Characteristics (Continued)

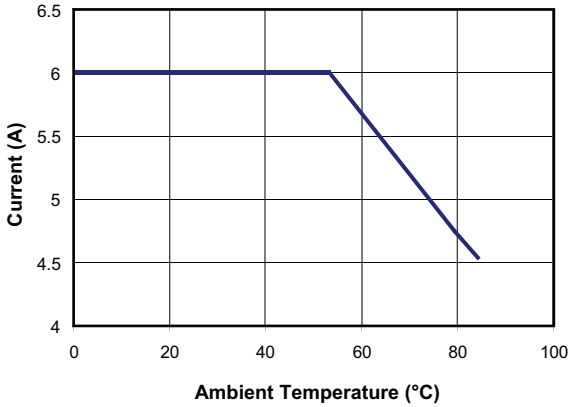
Enable Input Threshold (Rising) vs Temperature



Enable Input Threshold (Falling) vs. Temperature



Current Derating Curve @ 6A, V_{IN} = 12V



Detailed Description

Introduction

The AOZ1361DI is a 35mΩ P-channel high-side load switch with adjustable soft-start slew-rate control, programmable current limit and thermal shutdown. It operates with an input voltage range from 4.5V to 28V.

Enable

The EN pin is the ON/OFF control for the output switch. The device is enabled when EN pin is high and V_{IN} is above UVLO. The EN pin must be driven to a logic high or logic low state to guarantee operation. While disabled, the AOZ1361DI only draws about 1µA supply current.

Under-Voltage Lockout (UVLO)

The under-voltage lockout (UVLO) circuit of AOZ1361DI monitors the input voltage and prevents the output MOSFET from turning on until V_{IN} exceeds 3.9V.

Adjustable Soft-Start Slew-Rate Control

When the EN pin is asserted high, the slew rate control circuitry applies voltage on the gate of the PMOS switch in a manner such that the output voltage and current is ramped up linearly until it reaches the steady-state load current level. The slew rate can be adjusted by an external capacitor connected to the SS pin to ground. The slew rate rise time, Ton, can be set using the following equation:

$$Ton = \frac{Css \times V_{IN}}{30\mu A}$$

Programmable Current Limit

The current limit is programmed by an external resistor connected to the SET pin to ground. This sets a reference voltage to the current limit error amplifier that compares it to a sensed voltage that is generated by passing a small portion of the load current through an internal amplifier. When the sensed load current exceeds the set current limit, the load current is then clamped at the set limit and the Vout drop should be the result of resistance increasing. The AOZ1361DI will stay in this condition until the load current no longer exceeds the current limit or if the thermal shutdown protection is engaged. To set the current limit use Figure 3 on the following page.

Thermal Shut-down Protection

The thermal overload protection of AOZ1361DI is engaged to protect the device from damage should the die temperature exceeds safe margins due to a short circuit, extreme loading or heating from external sources.

1. **AOZ1361DI-01 (Auto-restart version):** During current limit or short circuit conditions, the PMOS resistance is increased to clamp the load current. This increases the power dissipation in the chip causing the die temperature to rise. When the die temperature reaches 130°C the thermal shutdown circuitry will shutdown the device. There is a 30°C hysterisis. The device will turn back on and go through soft start after the temperature drops below +100°C . The thermal shutdown will cycle repeatedly until the over temperature condition disappears or the enable pin is pulled LOW.
2. **AOZ1361DI-02 (Latch-off version):** Thermal shut-down protection sets a fault latch and shuts off the internal MOSFET and asserts the FLTB output if the junction temperature exceeds +130°C. The AOZ1361DI can be re-enabled by toggling EN pin after the die temperature drops below +100°C.

FLTB

The FLTB pin is an open drain output that is asserted low when either an over-current, short-circuit or over-temperature condition occurs. To prevent false alarm, the AOZ1361DI implements a fault delay time for over-temperature, over-current and short-circuit fault conditions. The FLTB pin becomes high impedance when the fault conditions are removed. For AOZ1361DI-02, if the temperature is higher than +130°C, the device will latch off. After that, if temperature drops below +100°C, the FLTB pin will pull high, which means the fault condition has already been removed, although there is no output voltage due to latch off function. A pull-up resistor must be connected between FLTB to 5V or 3.3V to provide a logic signal.

TFLT

TFLT is a fault delay pin, and its delay time is adjustable by a capacitor connected from TFLT to GND. The delay time can be calculated by:

C_{TLT} (µs) = 600 µs / nF x C_{TFLT} (nF)

Applications Information

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on and to limit input voltage drop. Also it is to prevent high-frequency noise on the power line from passing through the output of the power side. The choice of the input capacitor is based on its ripple current and voltage ratings rather than its capacitor value. The input capacitor should be located as close to the VIN pin as possible. A 1µF ceramic cap is recommended. However, higher capacitor values further reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1µF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transients. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

Current Limit Setting

The current limit is program by using external resistor connected to the SET pin. To set the current limit, use the Figure 3 below.

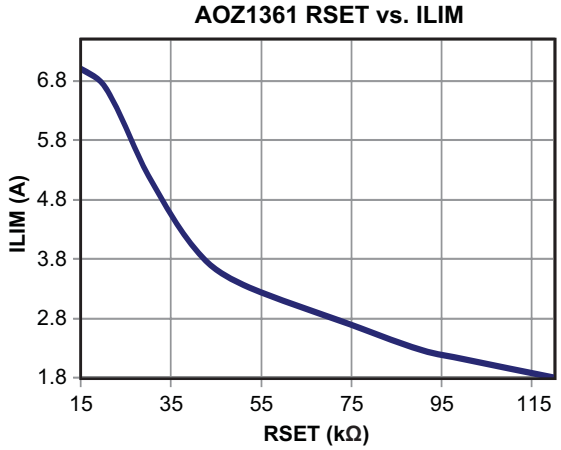


Figure 3. Current Limit vs. RSET (V_{IN} = 12V)

Slew Rate Setting

Slew rate is set by changing the capacitor value on the SS pin of the device. A capacitor connected between this SS pin and ground will reduce the output slew-rate. The capacitive range is 0.001µF to 0.1µF. See Figure 4 for Output Slew Rate Adjustment vs. Capacitance.

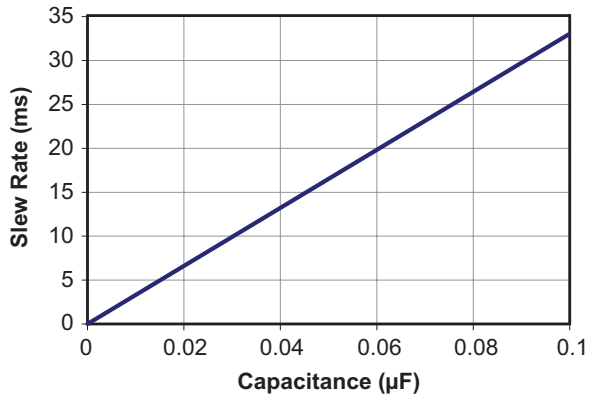


Figure 4. Output Slew Rate Adjustment vs. Capacitance

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$P_D = R_{ON} \times (I_{OUT})^2$$

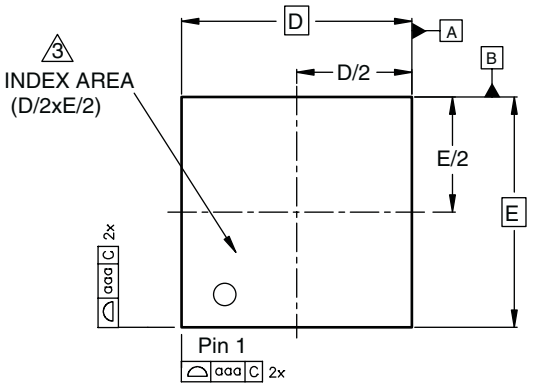
The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$$

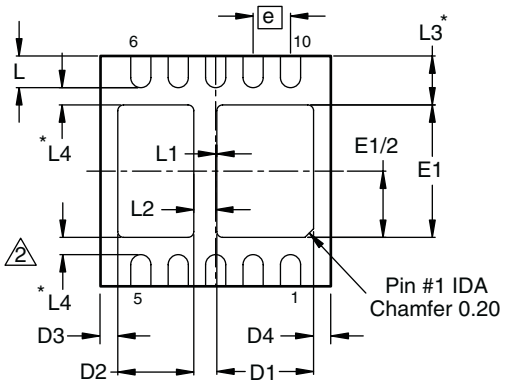
Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of AOZ1361. To optimize the switch response time to output short-circuit conditions keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

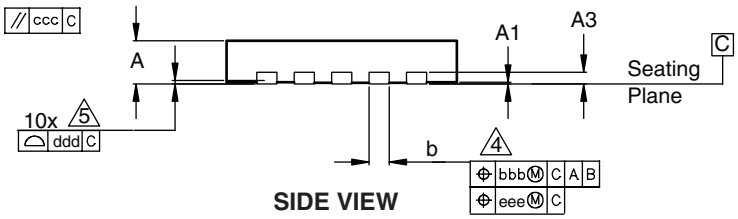
Package Dimensions, DFN 4x4



6 TOP VIEW

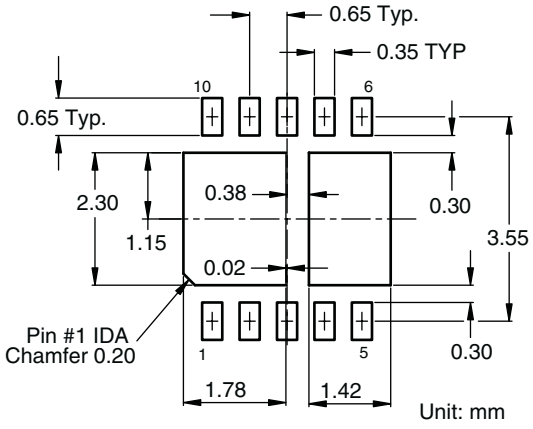


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.30	0.35	0.40
D	3.95	4.00	4.05
D1	1.58	1.68	1.78
D2	1.22	1.32	1.42
D3		0.3 REF	
D4		0.3 REF	
E	3.95	4.00	4.05
E1	2.20	2.30	2.40
e		0.65 BSC	
L	0.50	0.55	0.60
L1	—	0.02	0.12
L2	0.28	0.38	0.48
L3		0.85 REF	
L4		0.30 REF	
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.08	
eee		0.05	

Dimensions in inches

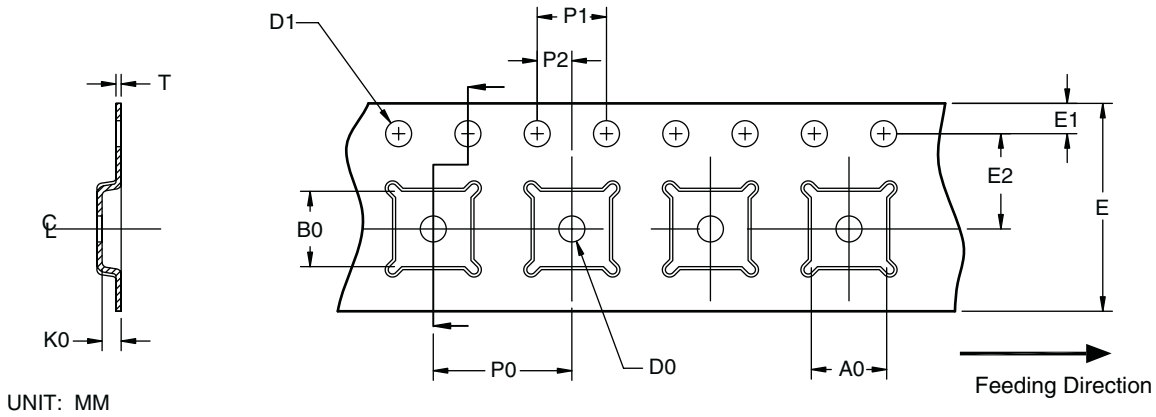
Symbols	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3		0.008 REF	
b	0.012	0.014	0.016
D	0.156	0.157	0.159
D1	0.062	0.066	0.070
D2	0.048	0.052	0.056
D3		0.012 REF	
D4		0.012 REF	
E	0.156	0.157	0.159
E1	0.087	0.091	0.094
e		0.026 BSC	
L	0.020	0.022	0.024
L1	—	0.001	0.005
L2	0.011	0.015	0.019
L3		0.033 REF	
L4		0.012 REF	
aaa		0.006	
bbb		0.004	
ccc		0.004	
ddd		0.003	
eee		0.002	

Notes:

1. All dimensions are in millimeters.
2. The dimensions with * are just for reference.
3. The location of the terminal #1 identifier and terminal numbering convention conforms to JEDEC publication 95 SPP-002.
4. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, then dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all other bottom surface metallization.
6. Drawings shown are for illustration only.

Tape and Reel Dimensions, DFN 4x4

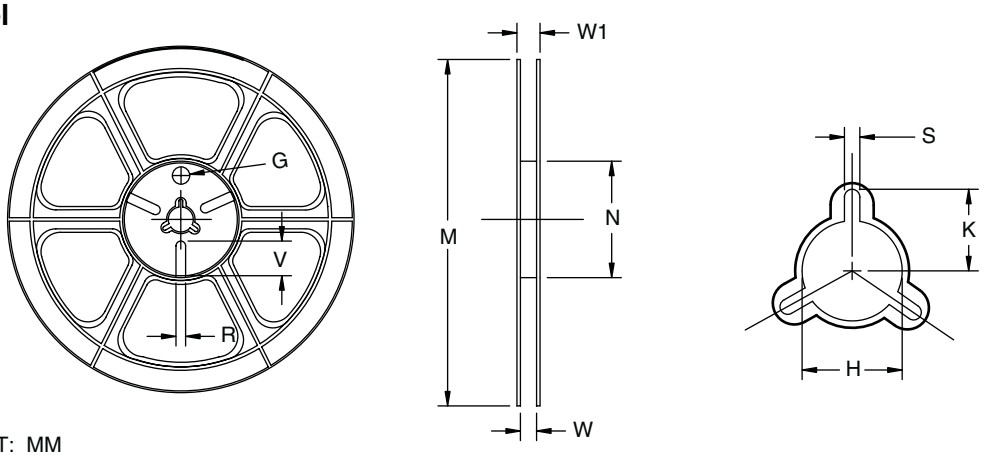
Carrier Tape



UNIT: MM

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 4x4 (12mm)	4.35 0.10	4.35 0.10	1.10 0.10	1.50 Min.	1.50 +0.1/-0.0	12.0 0.3	1.75 0.10	5.50 0.05	8.00 0.10	4.00 0.10	2.00 0.05	0.30 0.05

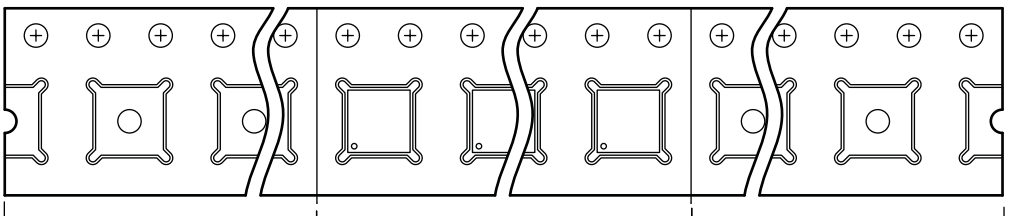
Reel



UNIT: MM

Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.0 2.0	ø79.0 1.0	12.4 +2.0/-0.0	17.0 +2.6/-0.0	ø13.0 0.5	10.5 0.2	2.0 0.5	—	—	—

Leader/Trailer and Orientation



Part Marking