TOSHIBA Bi-CMOS Integrated Circuit Silicon Monolithic

TB62802AFG

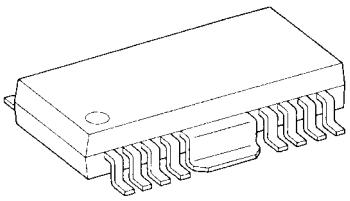
CCD Clock Drivers

The TB62802AFG is a clock distribution driver for CCD linear image sensors.

The IC can functionally drive the CCD input capacitance. It also supports inverted outputs, eliminating the need for cross point control.

The IC contains a 1-to-4 clock distribution driver and 4-bit buffer.

The suffix (G) appended to the part number represents a Lead (Pb) -Free product.



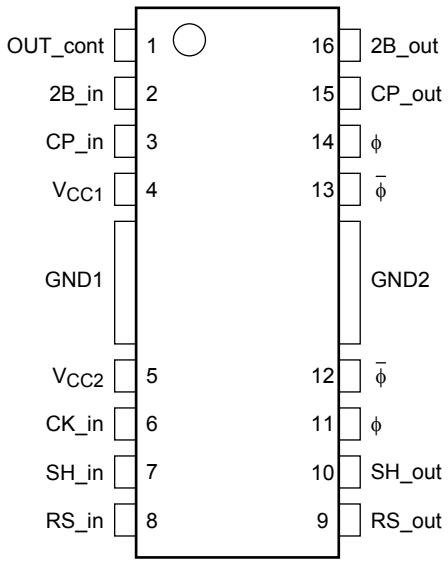
HSOP16-P-300-1.00

Weight: 0.5 g (typ.)

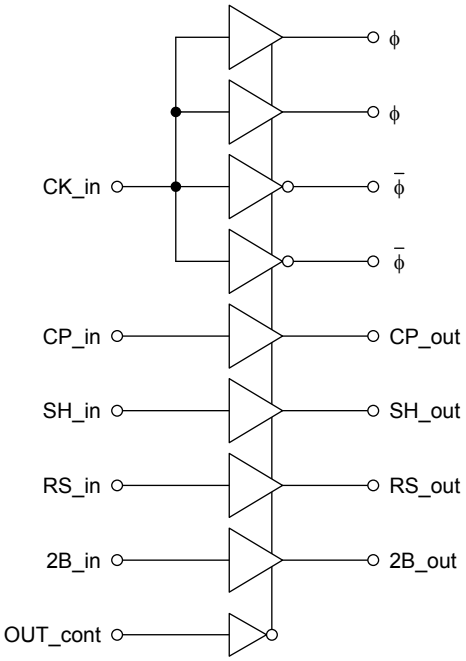
Features

- High drivability:
  In the case of 4-bit distribution driver ,
  Guaranteed driving 250 pF load capacitance @fclock = 25 MHz.
  In the case of 2-bit distribution driver (ϕ only or $\bar{\phi}$ only),
  Guaranteed driving 250 pF load capacitance @fclock = 35 MHz.
- Operating temperature range: Ta = 0°C to 60°C

Pin Connection (top view)



Logic Diagram



Pin Description

Pin No.	Pin Name	Functions	Remarks
1	OUT_cont	Output control pin	Internal pull down R=250 k ohm
2	2B_in	Light load drive input	Driver input for CCD last-stage clock
3	CP_in	Light load drive input	CCD clamp gate driver input
4	V_{CC1}	Light load power supply	—
—	GND1	Light load ground	—
5	V_{CC2}	Heavy load power supply	—
6	CK_in	Heavy load drive input	Driver input for CCD transfer clock
7	SH_in	Light load drive input	CCD shift gate driver input
8	RS_in	Light load drive input	CCD reset gate driver input
9	RS_out	Light load drive output (not inverted)	CCD reset gate driver output
10	SH_out	Light load drive output (not inverted)	CCD shift gate driver output
11	ϕ	Heavy load drive output (not inverted)	Driver output for CCD transfer clock
12	$\bar{\phi}$	Heavy load drive output (inverted)	Driver output for CCD transfer clock
—	GND2	Heavy load ground	—
13	$\bar{\phi}$	Heavy load drive output (inverted)	Driver output for CCD transfer clock
14	ϕ	Heavy load drive output (not inverted)	Driver output for CCD transfer clock
15	CP_out	Light load drive output (not inverted)	CCD clamp gate driver output
16	2B_out	Light load drive output (not inverted)	Driver output for CCD last-stage clock

Note1: The internal circuits for heavy load drive pins ϕ and $\bar{\phi}$ have the same configuration as those of light load drive pins RS_out, SH_out, CP_out and 2B_out. Thus, these internal circuits have the same characteristics.

Truth Table

Input				Output	
Pin Name	Logic	Pin Name	Logic	Pin Name	Logic
OUT_cont	L	CK_in	L	ϕ	L
				$\bar{\phi}$	H
			H	ϕ	H
				$\bar{\phi}$	L
		CP_in	L	CP_out	L
			H		H
		SH_in	L	SH_out	L
			H		H
		RS_in	L	RS_out	L
			H		H
		2B_in	L	2B_out	L
			H		H
	H	—	—	All Output	L

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Power supply voltage		V_{CC}	−0.3 to 6.0	V
Input voltage		V_{IN}	−0.3 to V_{CC} + 0.3	V
Output voltage		V_O	−0.5 to V_{CC}	V
Output current excluding other than ϕ, $\bar{\phi}$ outputs	High level	I_{OH} (O)	−16.0	mA
	Low level	I_{OL} (O)	+16.0	mA
ϕ output current	High level	I_{OH} (ϕ)	−150	mA
	Low level	I_{OL} (ϕ)	150	mA
Storage temperature		T_{stg}	−40 to 150	°C
Junction temperature		T_j	150	°C
Thermal resistance	Chip to ambient air	θ_{ja}	83	°C/W

Note2: Output current is specified as follows: V_{OH} = 4.0 V, V_{OL} = 0.5 V.

Operating Conditions (Ta = 25°C)

Characteristic		Symbol	Min	Typ.	Max	Unit
Power supply voltage		V_{CC}	4.7	5.0	5.5	V
Input voltage		V_{IN}	0	—	V_{CC}	V
Output voltage		V_O	0	—	V_{CC}	V
Output current excluding ϕ, $\bar{\phi}$ outputs	High level	I_{OH} (O)	—	—	−8.0	mA
	Low level	I_{OL} (O)	—	—	8.0	mA
ϕ output current	High level	I_{OH} (ϕ)	—	—	−10.0	mA
	Low level	I_{OL} (ϕ)	—	—	10.0	mA
Thermal resistance (chip to case)		θ_{jc}	—	12	—	°C/W
Operating temperature		T_{opr}	0	25	60	°C
Input rise/fall time	(Note3)	tri/tfi	—	2.5	5.0	ns

Note3: There is no hysteresis in the input block of this IC. Therefore attention should be given to the following:

A CMOS integrated circuit charges and discharges the capacitance load (internal equivalent capacitance) of the internal circuit while operating. The charged or discharged current flows in the package of the IC and inductance of transmission line, which causes inductive spike voltage to be generated.

When the spike voltage is generated in the reference GND, it affects the amplitude of an input signal. The amplitude seems to be fluctuating compared to when no spike voltage is generated in the reference GND. In this case, some induced spike waveforms exceed the input threshold level. For low-frequency inputs, the rate at which a spike exceeds the level increases, resulting in unstable output.

Therefore, do not apply input signals lower than 1 μs. When designing a board, be sure to take transmission line inductance into consideration.

Electrical Characteristics

DC Characteristics (unless otherwise specified, V_{CC} = 4.7 to 5.5 V, Ta = 0 to 60°C)

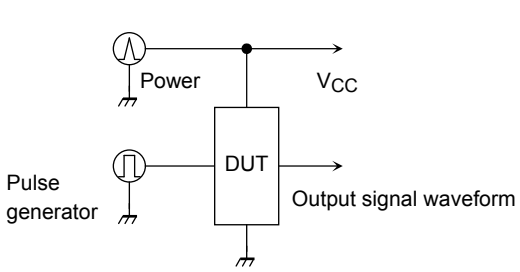
Characteristic		Symbol	Test Circuit	Test Condition	V_{CC}	Min	Typ.	Max	Unit
Input voltage	High	V_{IH}	1		4.7	2.0	—	V_{CC}	V
	Low	V_{IL}			4.7	0	—	0.8	
Output voltage excluding ϕ, $\bar{\phi}$ outputs		V_{OH} (O)	2	I_{OH} = –50 μA	4.7	4.5	—	V_{CC}	V
				I_{OH} = –8 mA	4.7	3.9	—	V_{CC}	
		V_{OL} (O)	4	I_{OL} = 50 μA	4.7	0	—	0.2	
				I_{OL} = 8 mA	4.7	0	—	0.7	
ϕ output voltage		V_{OH} (ϕ/$\bar{\phi}$)	2,3	I_{OH} = –10 mA	4.7	4.5	—	V_{CC}	V
				I_{OH} = –30 mA	4.7	3.9	—	V_{CC}	
				I_{OH} = –120 mA	4.7	3.0	—	V_{CC}	
		V_{OL} (ϕ/$\bar{\phi}$)	4,5	I_{OL} = 50 μA	4.7	0	—	0.3	
				I_{OL} = 30 mA	4.7	0	—	0.5	
				I_{OL} = 120 mA	4.7	0	—	2.0	
Input voltage		I_{IN1}	6	V_{IN} (2,3,6,7,8pin) = V_{CC} or GND	5.5	–1.0	—	1.0	μA
		I_{IN2}		$V_{IN(1pin)}$ = V_{CC} or GND	5.5	—	—	35	
Static current consumption	Total	I_{CC}	7	For light load output, all bits are High. For heavy load output, 2 bits are High. 2 bits are Low.	5.5	—	—	15.0	mA
	Forced low for all bits	I_{CCL}	—	Out_cont = "H"	5.5	—	—	30.0	
	Each bit	ΔI_{CC}	8	One input : V_{IN} = 0.5 V or V_{CC} – 2.1 V Other inputs : V_{IN} = V_{CC} or GND	—	—	—	1.5	
Output off mode supply voltage		V_{POR}	(Note 4)	Light load power supply (V_{CC1}) reference	—	—	3.0	—	V

Note4: Refer to the description of the P.O.R below.

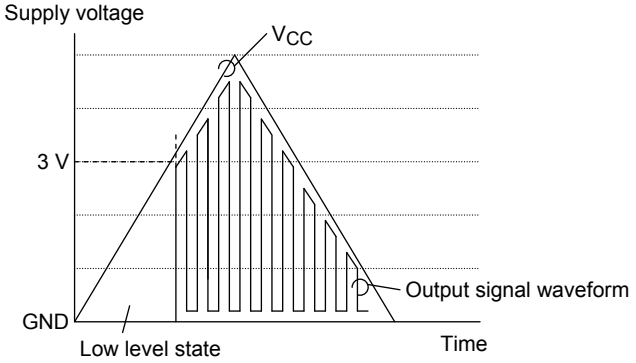
Mode in Which Output Is Held at Low at Power-On (P.O.R: Power On Reset circuit)

To eliminate the unstable period for the internal logic, this IC incorporates a function for monitoring the light load power supply (V_{CC1}) at power-on to maintain the outputs at Low.

- At power-on, all output are held at Low until light load power supply (V_{CC1}) reaches the voltage level of 3 V.
- When the light load power supply (V_{CC1}) voltage is higher than 3 V (typ.), the internal logic operates according to input signals.
- For normal operation, be sure to use a power supply of 4.7 V or higher as guaranteed.



P.O.R test circuit



Refer to Subsection 10. "Propagation Delay Time" in AC Parameters.

AC Characteristics (input transition rise or fall time: t_r/t_f = 3.0 ns)

Characteristic	Symbol	Test Condition	Ta = 25°C, V_{CC} = 5.0 V			Ta = 0 to 60°C V_{CC} = 4.7 to 5.5 V		Unit	Reference Measurement Diagram
			Min	Typ.	Max	Min	Max		
Propagation delay time	tpLH (ϕ)	C_L = 250 pF	—	10.8	—	5	16	ns	Measurement diagram 1
	tpHL (ϕ)		—	9.8	—	5	16		
	tpLH (O)	C_L = 20 pF	—	6.0	—	2	10		Measurement diagram 2
	tpHL (O)		—	6.2	—	2	12		
Output OFF time	tpCLH (ϕ)	C_L = 250 pF	—	11.5	—	5	19	ns	Measurement diagram 3
	tpCHL (ϕ)		—	10.5	—	5	19		
	tpCLH (O)	C_L = 20 pF	—	8.5	—	2	19		Measurement diagram 4
	tpCHL (O)		—	12.0	—	2	23		
Light load drive output skew	to (skw)	C_L = 20 pF	0	—	2.0	0	2.0	ns	Measurement diagram 5
Heavy load drive output crosspoints	VT (crs)	C_L = 100 to 250 pF	1.5	—	—	1.5	—	V	Measurement diagram 6
Equivalent internal capacitance (Note5)	CPD (ϕ)		—	32	—	—	—	pF	
	CPD (O)		—	9.4	—	—	—		

Note 5: CPD denotes “power dissipation capacitance”. Dynamic power dissipation can be calculated using the CPD value.

$$Pd = \Sigma [CPD \times V_{CC}^2 \times Fin] + \Sigma (CL \times V_{CC}^2 \times Fout)$$

CL: Load capacitance per output
CPD: Power dissipation capacitance
Fin: Input clock frequency
Fout: Output clock frequency

For example:
For heavy load drive output, driving a load capacity of 250 pF at 25 MHz;
For light load drive output, driving a load capacity of 20 pF at 25 MHz.

Note 6: In practice, the frequencies of some shift gate control signals are lower than the transfer clock. Therefore the power dissipation during practical use is smaller than the calculated value below.

$$Pd = [32\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz] \times 4\ bit + (250\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz) \times 4\ bit$$
$$+ [9.4\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz] \times 4\ bit + (20\ pF \times 5.0\ V \times 5.0\ V \times 25\ MHz) \times 4\ bit$$
$$\simeq 778\ mW$$

The typical power dissipation is approximately 778 mW.

Notes on System Design

As shown above, the TB62802AFG consumes high current while operating. There is temporary flow of a current greater than the calculated value. To suppress bouncing from the power supply and GND, decoupling for the power supply is a vital necessity.

Below is an example of how the capacitance of a decoupling capacitor is calculated. Be sure to refer to this when designing a system.

The decoupling capacitor should be placed underneath the IC to reduce the high-frequency components.

Supply current variable: 350 mA (estimated variable in 1 bit)
Supply voltage variable: 0.3 V
Noise pulse width: 10 ns (time in which fluctuation occurs)

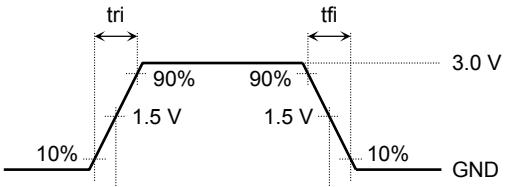
$$C = \Delta I_{CC}/(\Delta V/\Delta T)$$
$$= 350\ mA \times 4\ bit/(0.3\ V/10\ ns)$$
$$\simeq 47\ nF$$
$$\simeq 0.047\ \mu F \text{ (when using a normal capacitor)}$$

To control the fluctuation in the low-frequency components, it is recommended that the power supply on the board be decoupled using a 10 μF to 50 μF capacitor.

Waveform Measuring Point

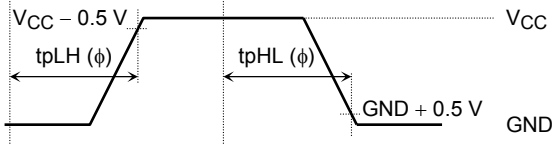
Propagation Delay Time Setting

Input signal
- 2B_in
- CK_in
- SH_in
- RS_in
- CP_in
- out_cont=L

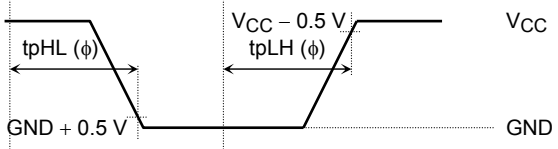


Measurement Diagram 1

- ϕ Output signal

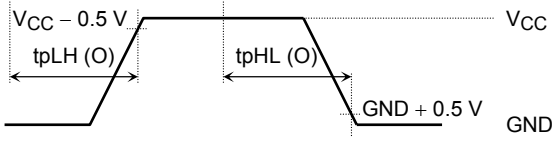


- $\bar{\phi}$ Output signal

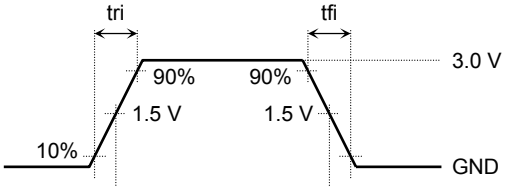


Measurement Diagram 2

- 2B_out
- CK_out
- SH_out
- RS_out
- CP_out



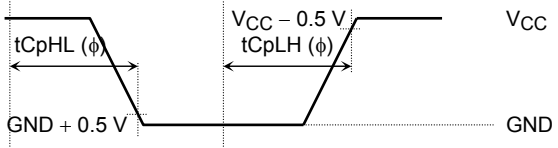
Input signal
- 2B_in＝CK_in＝SH_in＝RS_in＝CP_in＝H



- out_cont

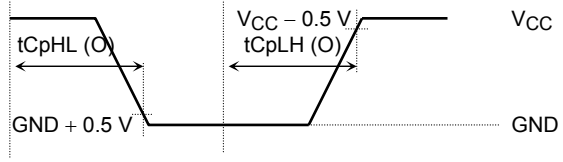
Measurement Diagram 3

- ϕ Output signal



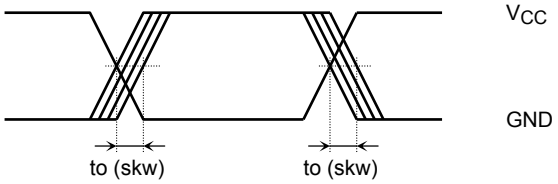
Measurement Diagram 4

- 2B_out
- CK_out
- SH_out
- RS_out
- CP_out



Measurement Diagram 5

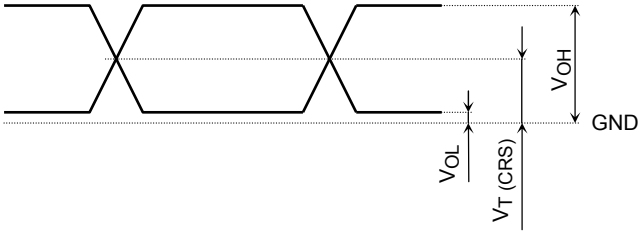
- 2B_out
- CK_out
- SH_out
- RS_out
- CP_out



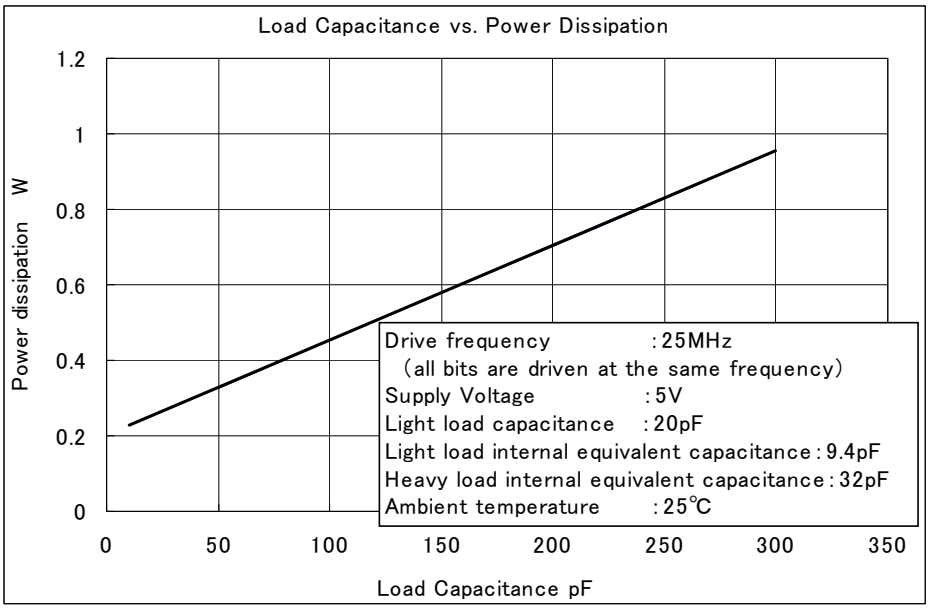
Output Waveform Crosspoint/Level Setting

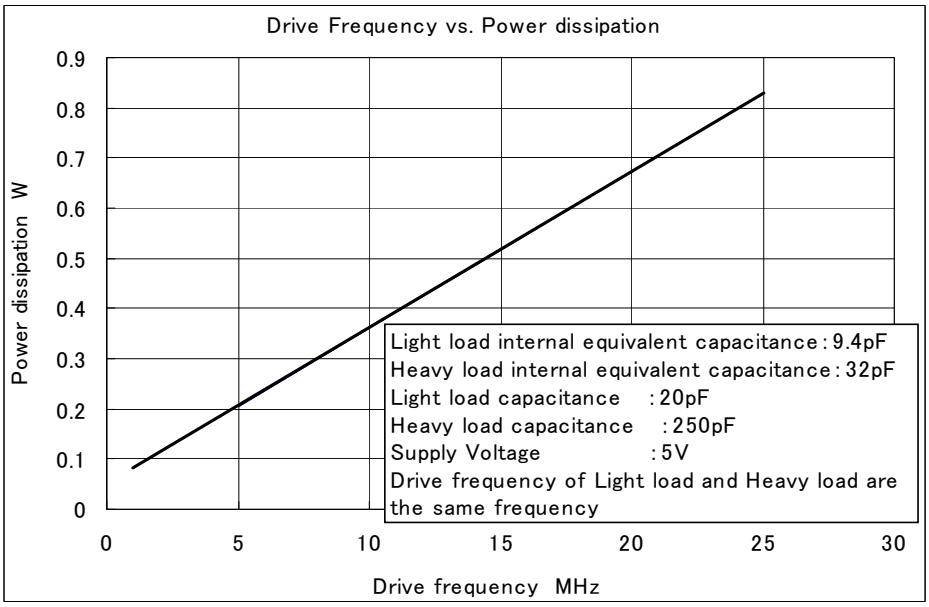
Measurement Diagram 6

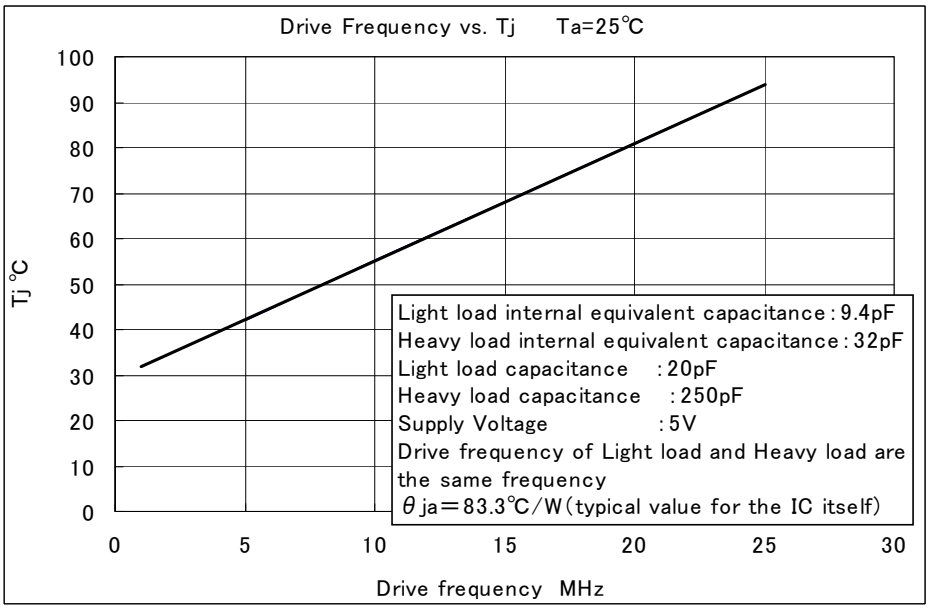
- ϕ Output signal
- $\overline{\phi}$ Output signal

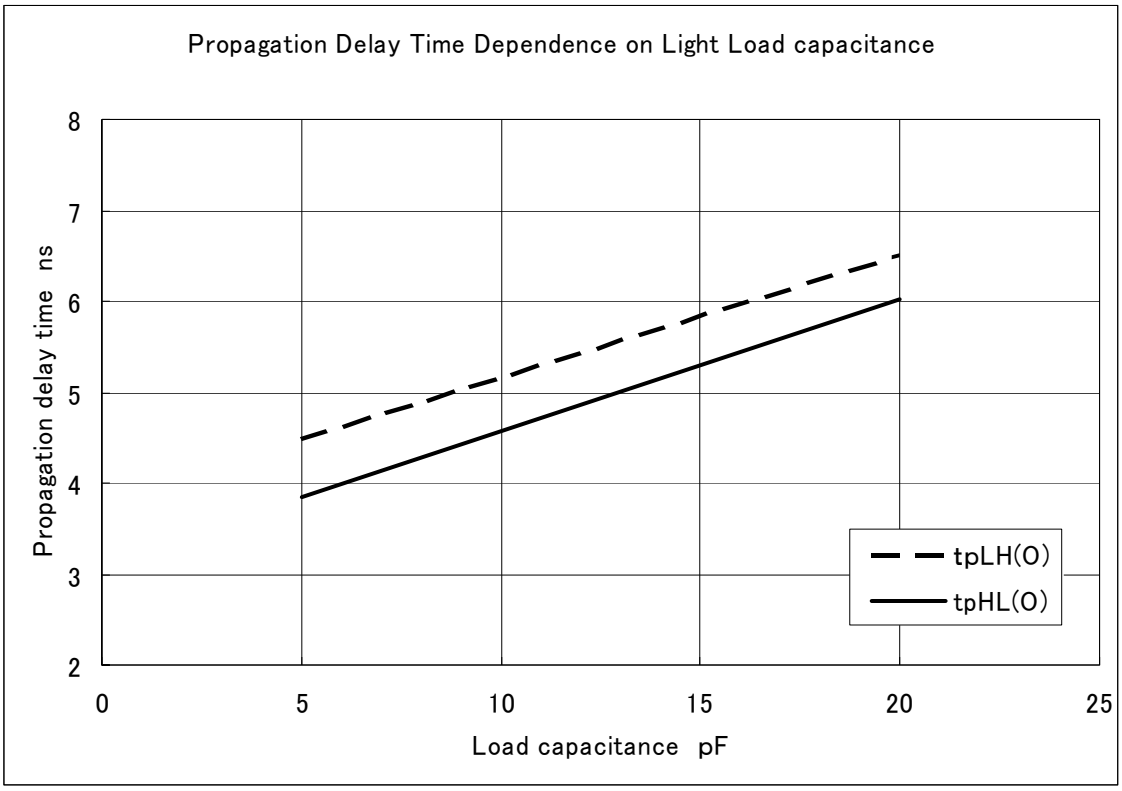


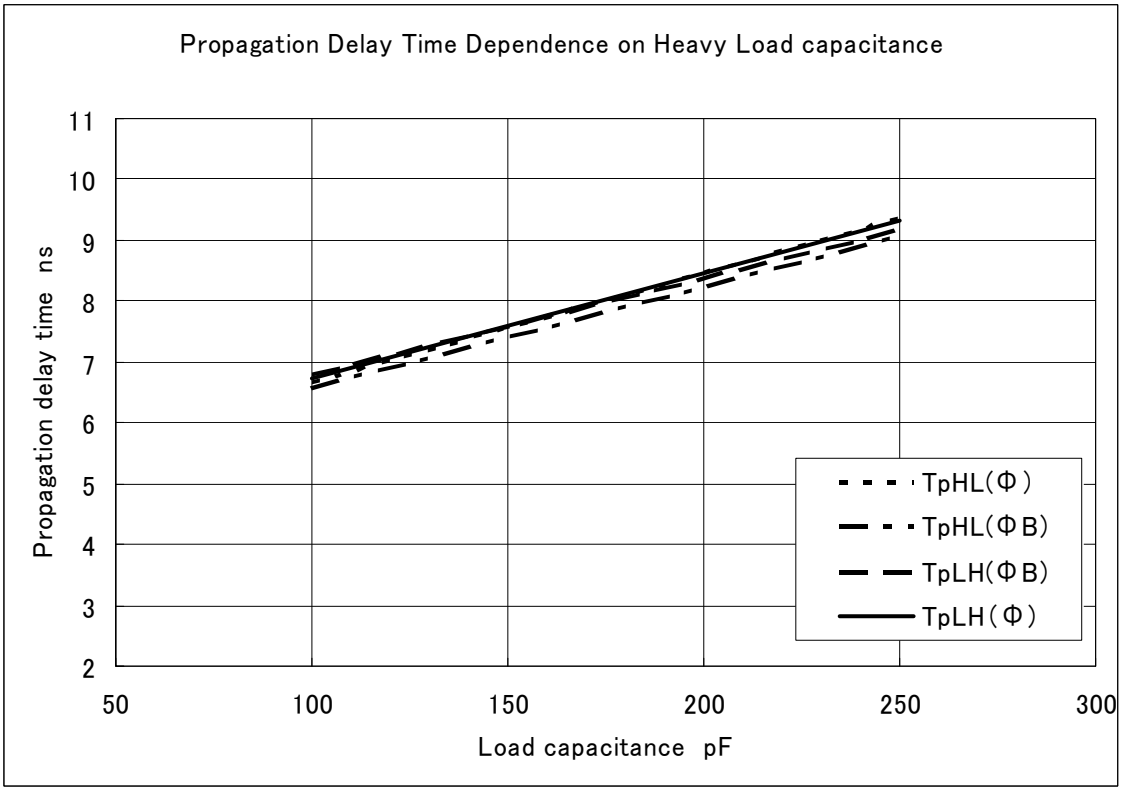
Reference Characteristics








Propagation Delay Time Dependence on Light Load capacitance
Propagation delay time ns
8
7
6
5
4
3
2
0
5
10
15
20
25
Load capacitance pF
tpLH(O)
tpHL(O)


Propagation Delay Time Dependence on Heavy Load capacitance
Propagation delay time ns
11
10
9
8
7
6
5
4
3
2
50
100
150
200
250
300
Load capacitance pF
TpHL(Φ)
TpHL(ΦB)
TpLH(ΦB)
TpLH(Φ)

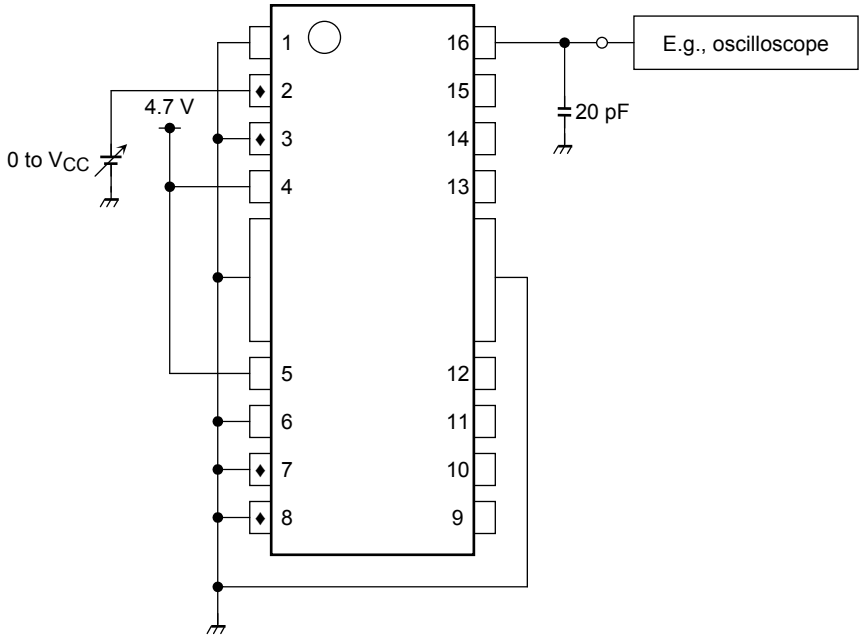
Test Circuit

DC Parameters

Pins marked with an asterisk (♦) are test pins. Be sure to ground those input pins that are not used as test pins so that the logic is determined. Unless otherwise specified, bits of the same type are measured in the same way.

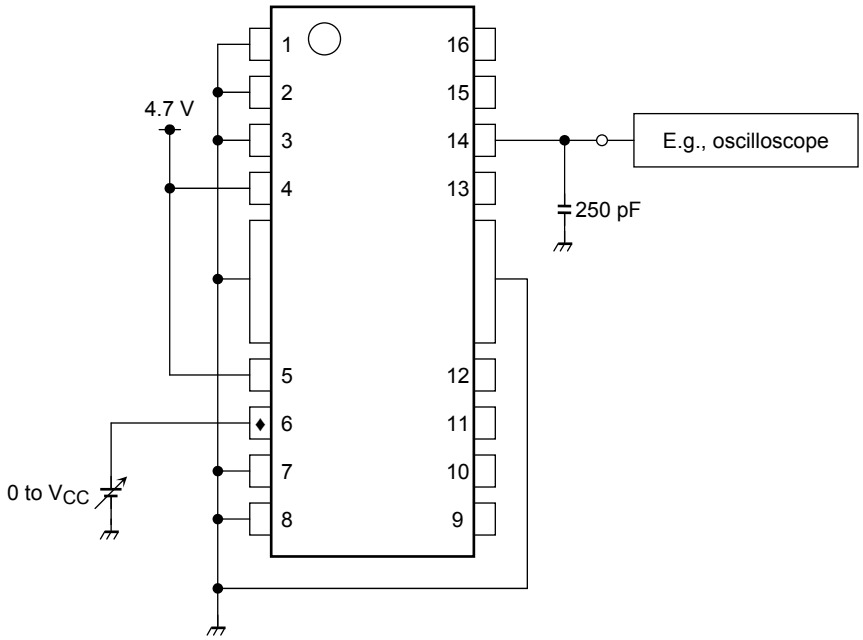
1. V_{IH}/V_{IL}

(1) Light load drive bits



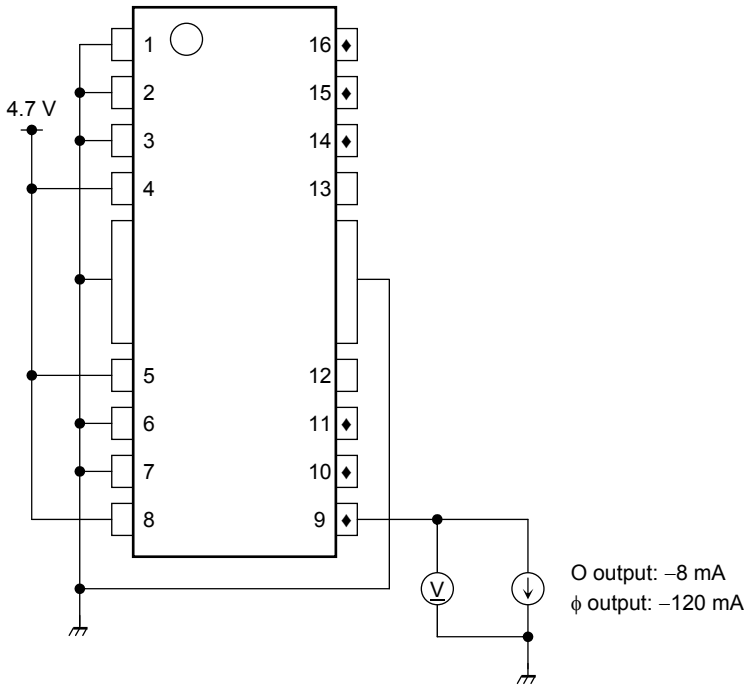
Note 7: When measuring input pins, connect to GND those input pins that are not being measured.

(2) Heavy load drive bits



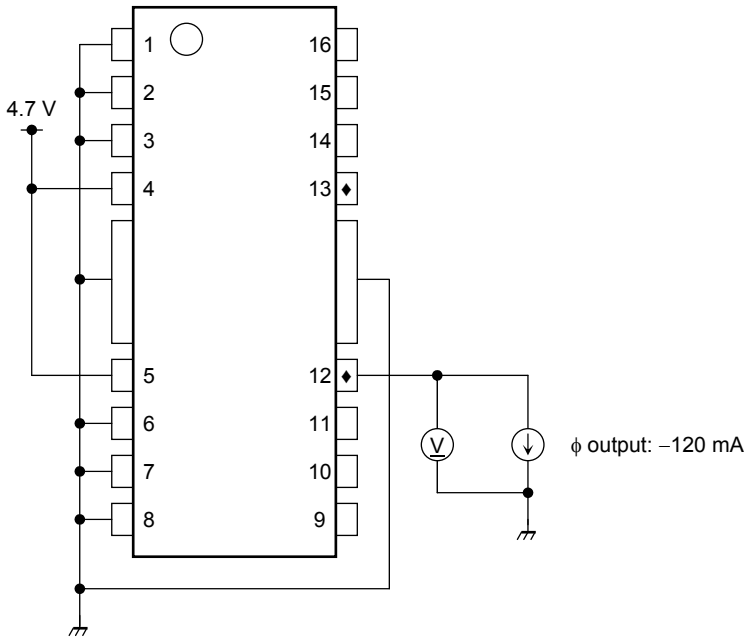
Note 8: Connect to GND those input pins that are not being measured.

2. V_{OH} (O/ϕ)



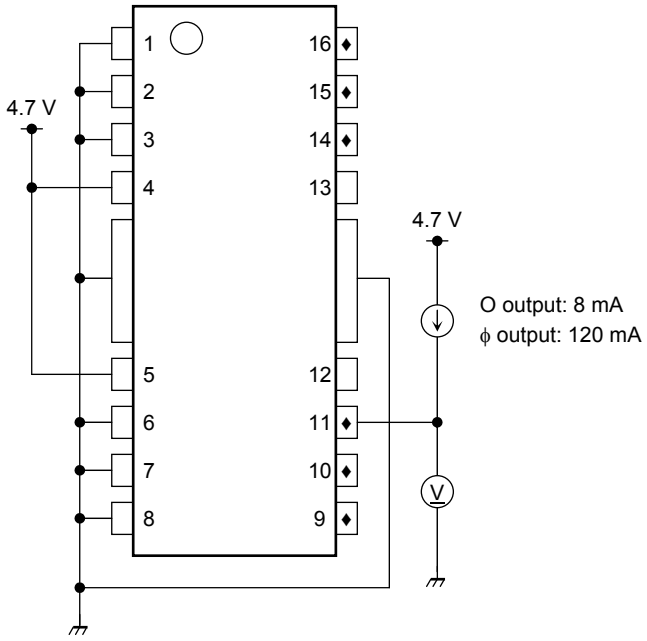
Note 9: Connect to GND those input pins that are not being measured.

3. V_{OH} ($\bar{\phi}$)



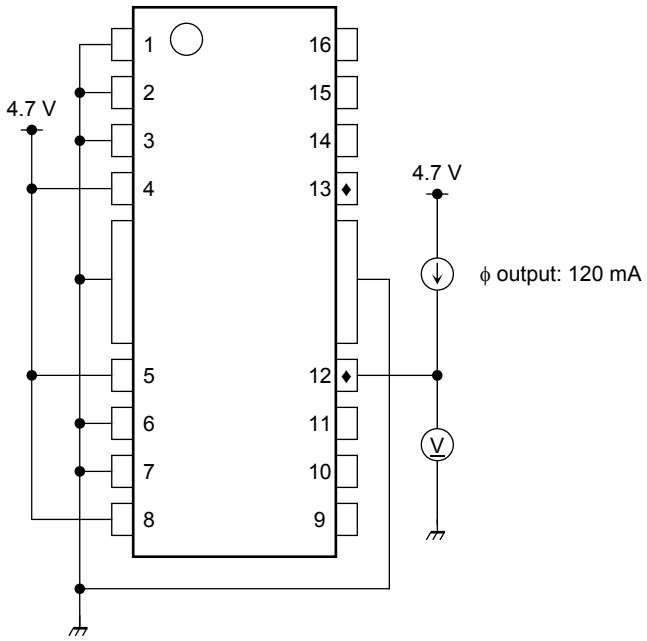
Note 10: Connect to GND those input pins that are not being measured.

4. V_{OL} (O/ϕ)



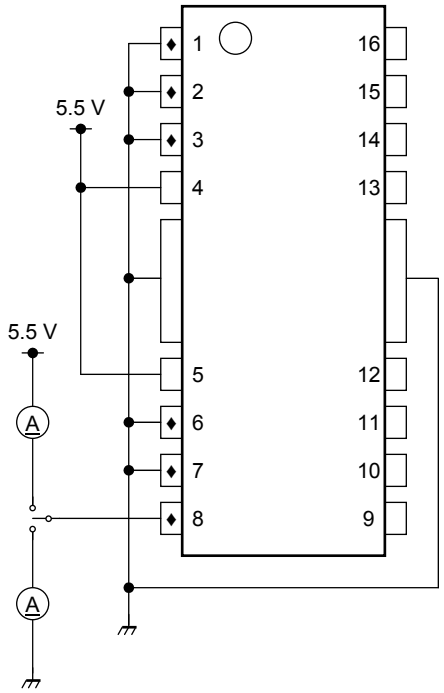
Note 11: Connect to GND those input pins that are not being measured.

5. V_{OL} ($\overline{\phi}$)



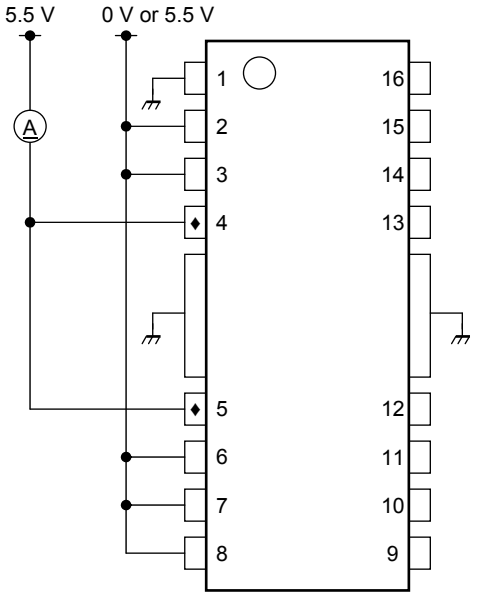
Note12: Connect to GND those input pins that are not being measured.

6. I_{IN}



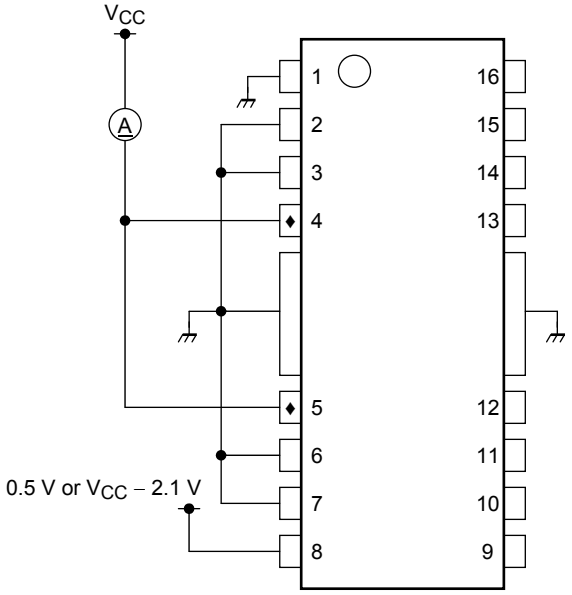
Note13: Connect to GND those input pins that are not being measured.

7. I_{CC}



Note 14: The input logic of the heavy load drive clock input pin (pin 6) is the same for HIGH or LOW.

8. ΔI_{CC}



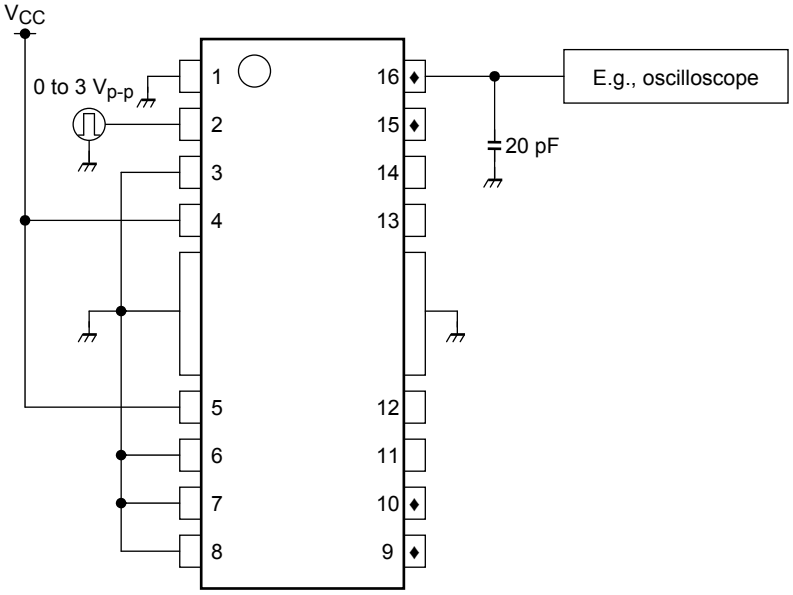
Note 15: When measuring input pins, connect to GND (or to the power supply) those input pins that are not being measured.

AC Parameters

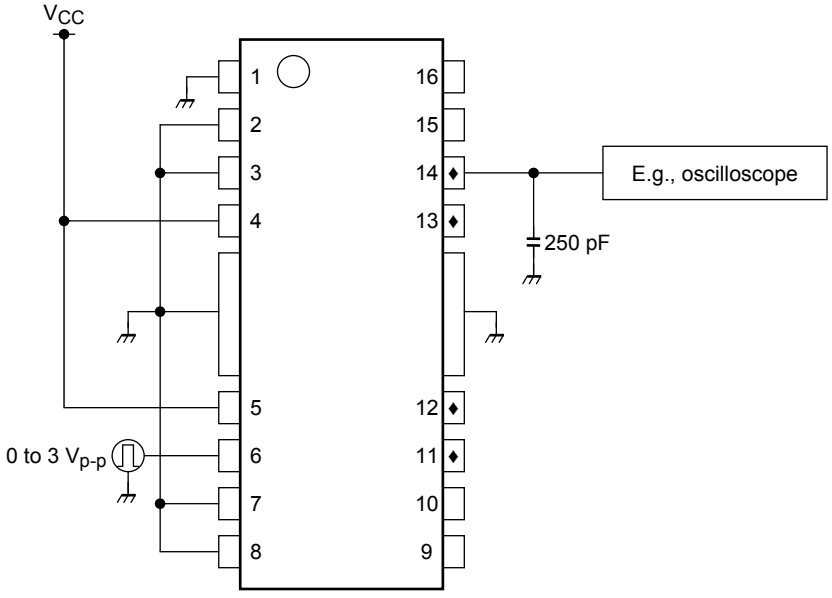
Pins marked with an asterisk (*) are test pins. Ground those input pins that are not being used as test pins so that the logic is determined. Unless otherwise specified, bits of the same type are measured in the same way.

9. Propagation Delay Time

(1) Light load drive bits

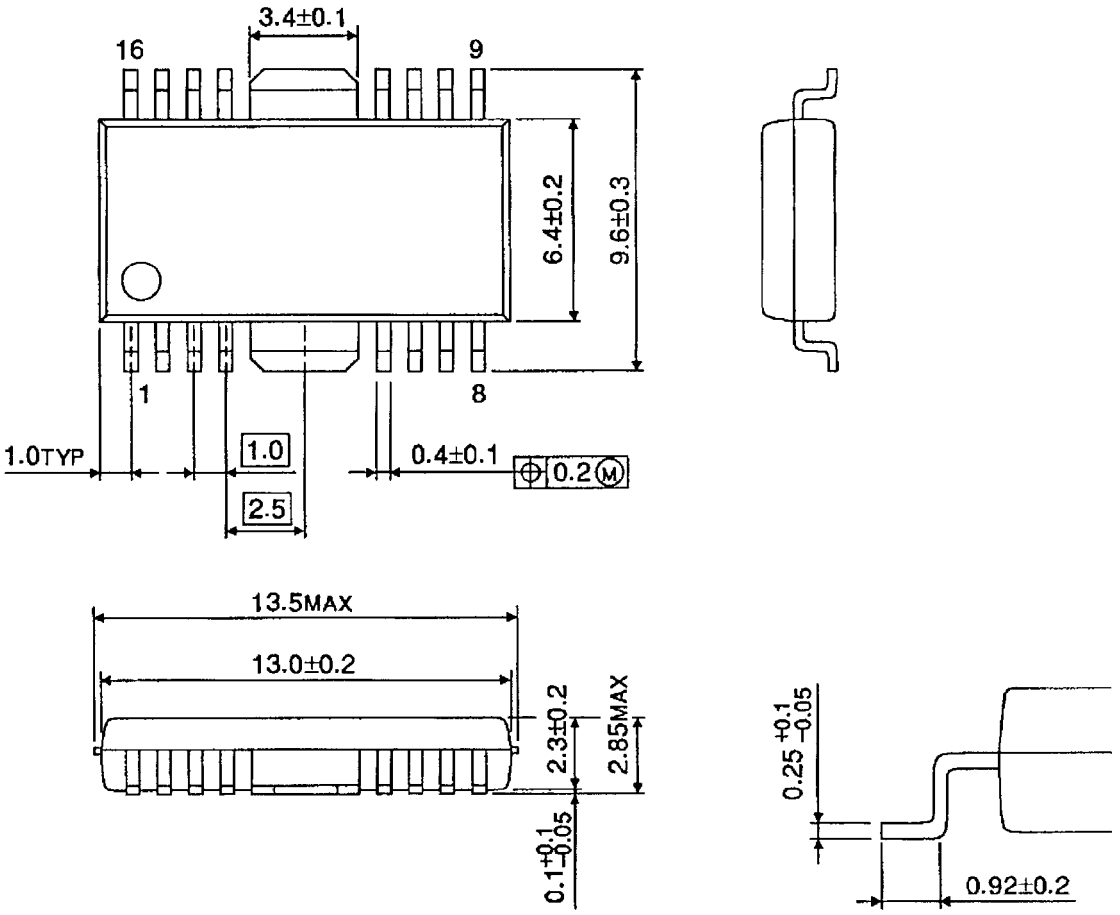


(2) Heavy load drive bits



Package Dimensions

HSOP16-P-300-1.00 Unit : mm



Weight: 0.5 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only.
Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

(5) Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.
If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, over current or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Points to Remember on Handling of ICs

(1) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(2) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

About solder ability, following conditions were confirmed

- Solder ability

(1) Use of Sn-37Pb solder Bath
- solder bath temperature = 230°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

(2) Use of Sn-3.0Ag-0.5Cu solder Bath
- solder bath temperature = 245°C
- dipping time = 5 seconds
- the number of times = once
- use of R-type flux

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