

SI4800

N-channel TrenchMOS™ logic level FET

Rev. 02 — 17 February 2004

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

1.2 Features

- Low gate charge
- Low on-state resistance
- Surface mounted package
- Fast switching.

1.3 Applications

- Portable appliances
- Lithium-ion battery chargers
- Notebook computers
- DC-to-DC converters.

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 9 \text{ A}$
- $P_{tot} \leq 2.5 \text{ W}$
- $R_{DSon} \leq 18.5 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT96-1 (SO-8), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)	<p>Top view MBK187</p>	<p>MBB076</p>
4	gate (g)		
5,6,7,8	drain (d)		

SOT96-1 (SO8)



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3. Ordering information

Table 2: Ordering information

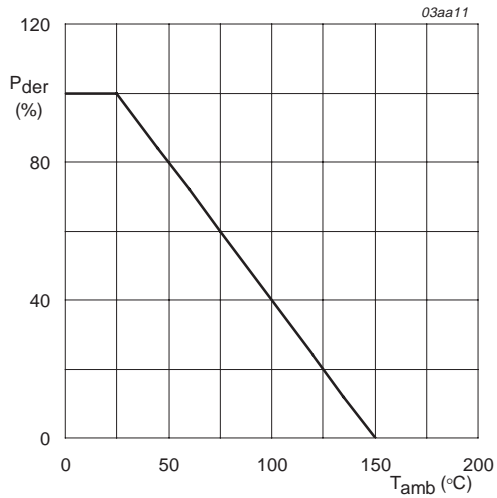
Type number	Package		Version
	Name	Description	
SI4800	SO8	plastic small outline package; 8 leads	SOT96-1

4. Limiting values

Table 3: Limiting values

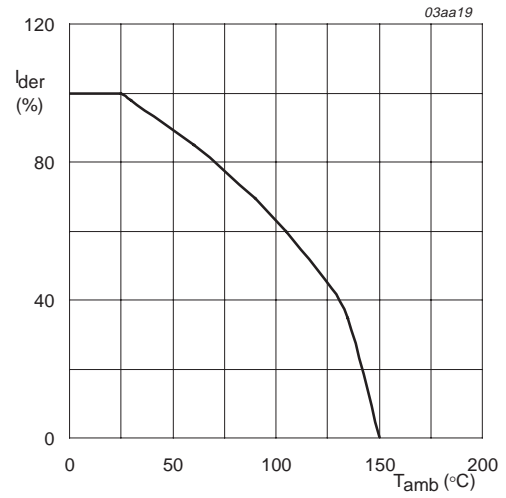
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 2 and 3	-	9	A
		$T_{amb} = 70\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 2	-	7	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	40	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 1	-	2.5	W
		$T_{amb} = 70\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$; Figure 1	-	1.6	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current	$T_{amb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ s}$	-	2.3	A



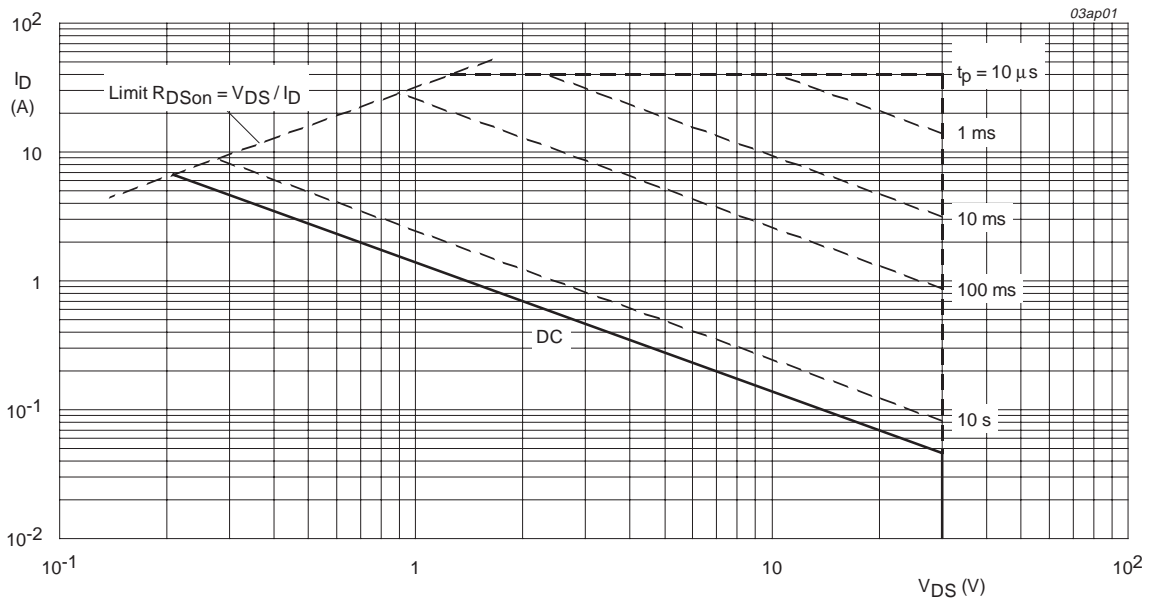
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of ambient temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of ambient temperature.



T_{amb} = 25 °C; I_{DM} is single pulse.

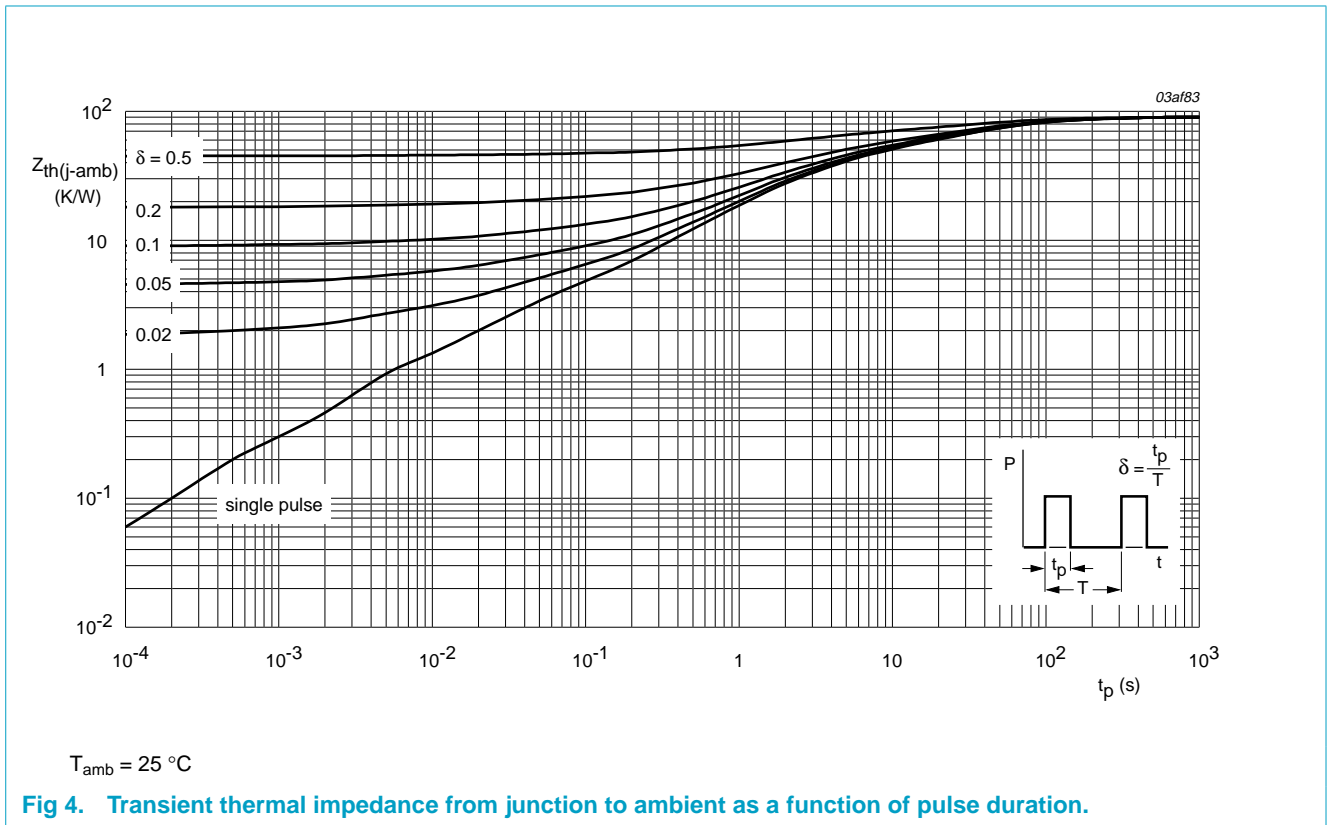
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; $t_p \leq 10$ s; Figure 4	-	-	50	K/W

5.1 Transient thermal impedance

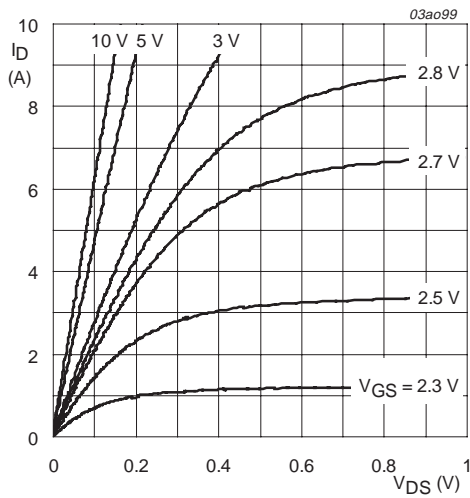


6. Characteristics

Table 5: Characteristics

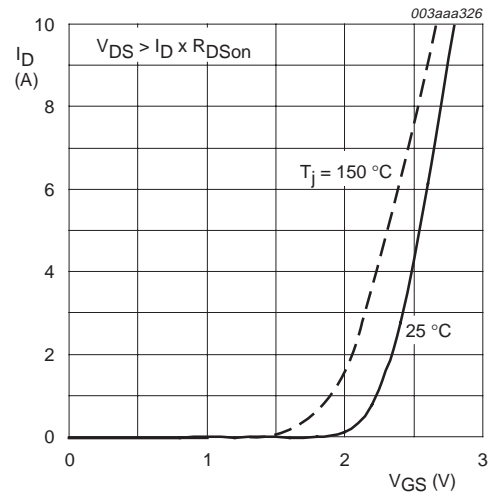
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 250\ \mu\text{A}$; $V_{DS} = V_{GS}$; Figure 9	0.8	-	-	V
I_{DSS}	drain-source leakage current	$V_{DS} = 24\ \text{V}$; $V_{GS} = 0\ \text{V}$	-	-	1	μA
		$T_j = 25\text{ °C}$	-	-	5	μA
		$T_j = 55\text{ °C}$	-	-	5	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0\ \text{V}$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ \text{V}$; $I_D = 9\ \text{A}$; Figure 7 and 8	-	15.5	18.5	$\text{m}\Omega$
		$V_{GS} = 4.5\ \text{V}$; $I_D = 7\ \text{A}$; Figure 7	-	24	33	$\text{m}\Omega$
$I_{D(on)}$	on-state drain current	$V_{DS} \geq 5\ \text{V}$; $V_{GS} = 10\ \text{V}$	30	-	-	A
Dynamic characteristics						
g_{fs}	forward transconductance	$V_{DS} = 15\ \text{V}$; $I_D = 9\ \text{A}$	-	19	-	S
$Q_{g(tot)}$	total gate charge	$I_D = 8\ \text{A}$; $V_{DD} = 15\ \text{V}$; $V_{GS} = 5\ \text{V}$; Figure 13	-	11.8	-	nC
Q_{gs}	gate-source charge		-	2.7	-	nC
Q_{gd}	gate-drain (Miller) charge		-	5	-	nC
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\ \text{V}$; $I_D = 1.5\ \text{A}$; $V_{GS} = 10\ \text{V}$; $R_G = 6\ \Omega$	-	6	16	ns
t_r	rise time		-	7	15	ns
$t_{d(off)}$	turn-off delay time		-	23	30	ns
t_f	fall time		-	11	15	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 7\ \text{A}$; $V_{GS} = 0\ \text{V}$; Figure 12	-	0.86	1.2	V
t_{rr}	reverse recovery time	$I_S = 7\ \text{A}$; $di_S/dt = -100\ \text{A}/\mu\text{s}$; $V_R = 30\ \text{V}$; $V_{GS} = 0\ \text{V}$	-	25	80	ns



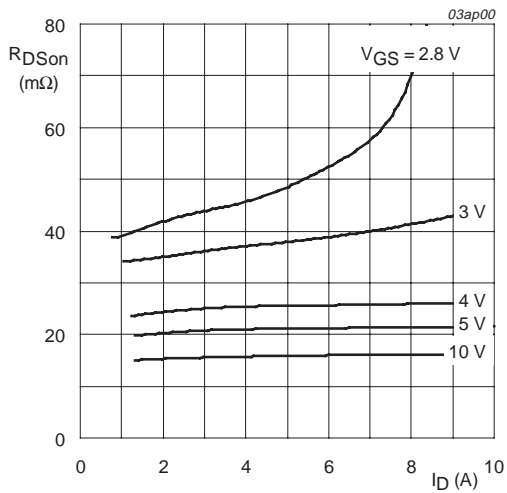
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



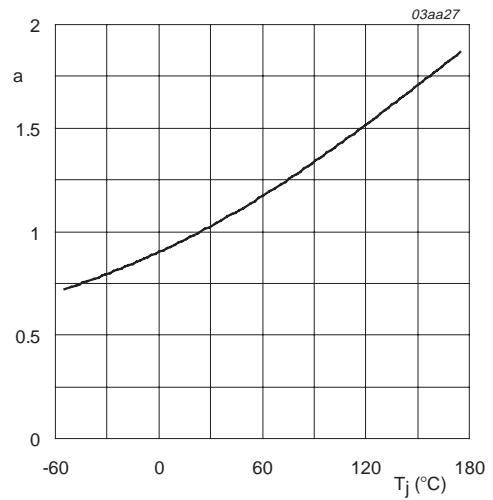
$T_j = 25^\circ\text{C}$ and 150°C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



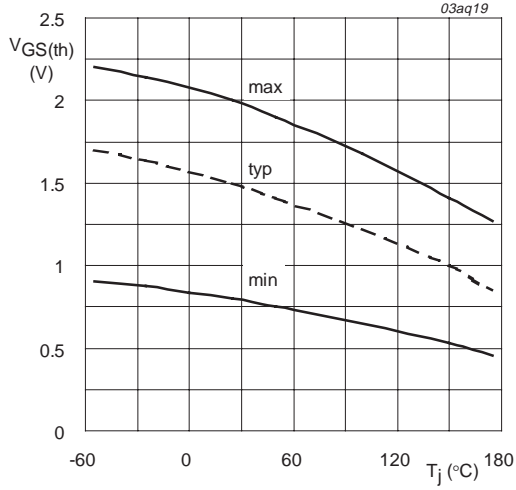
$T_j = 25^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



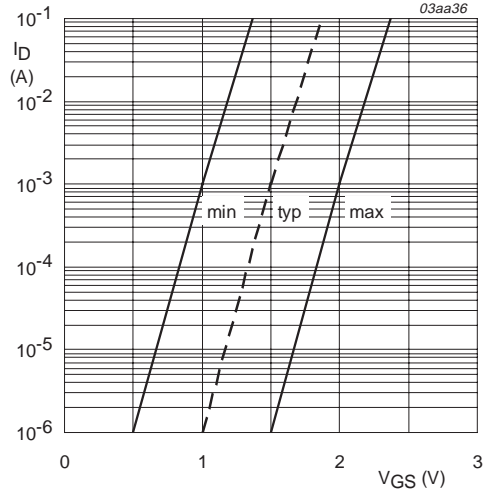
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



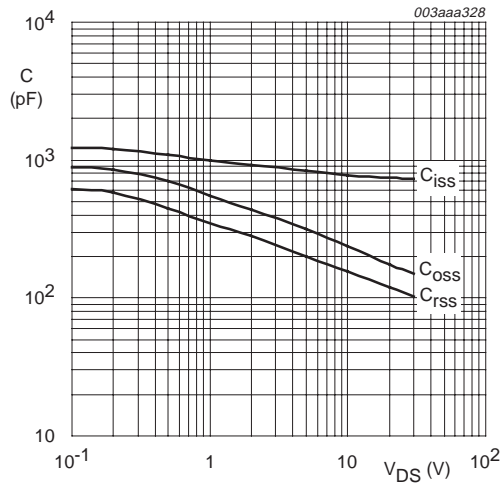
$I_D = 250 \mu A; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



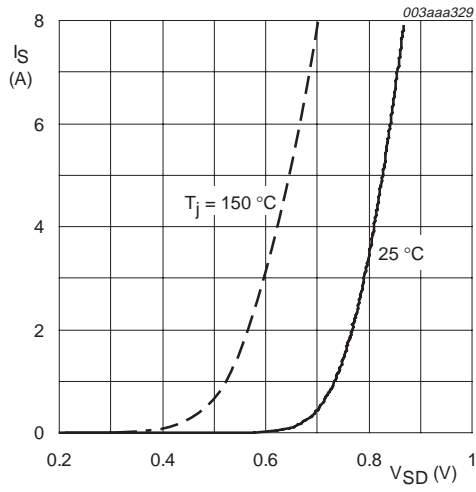
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



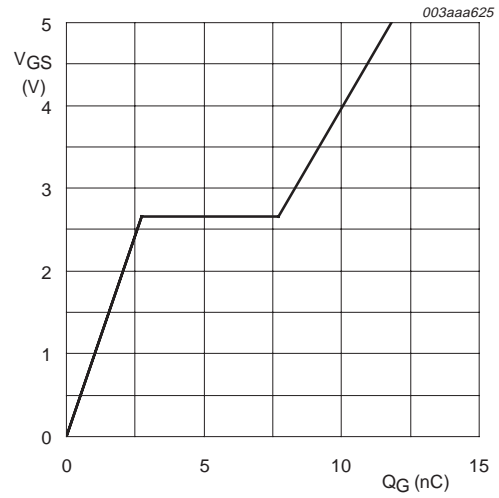
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 8\text{ A}$; $V_{DD} = 15\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

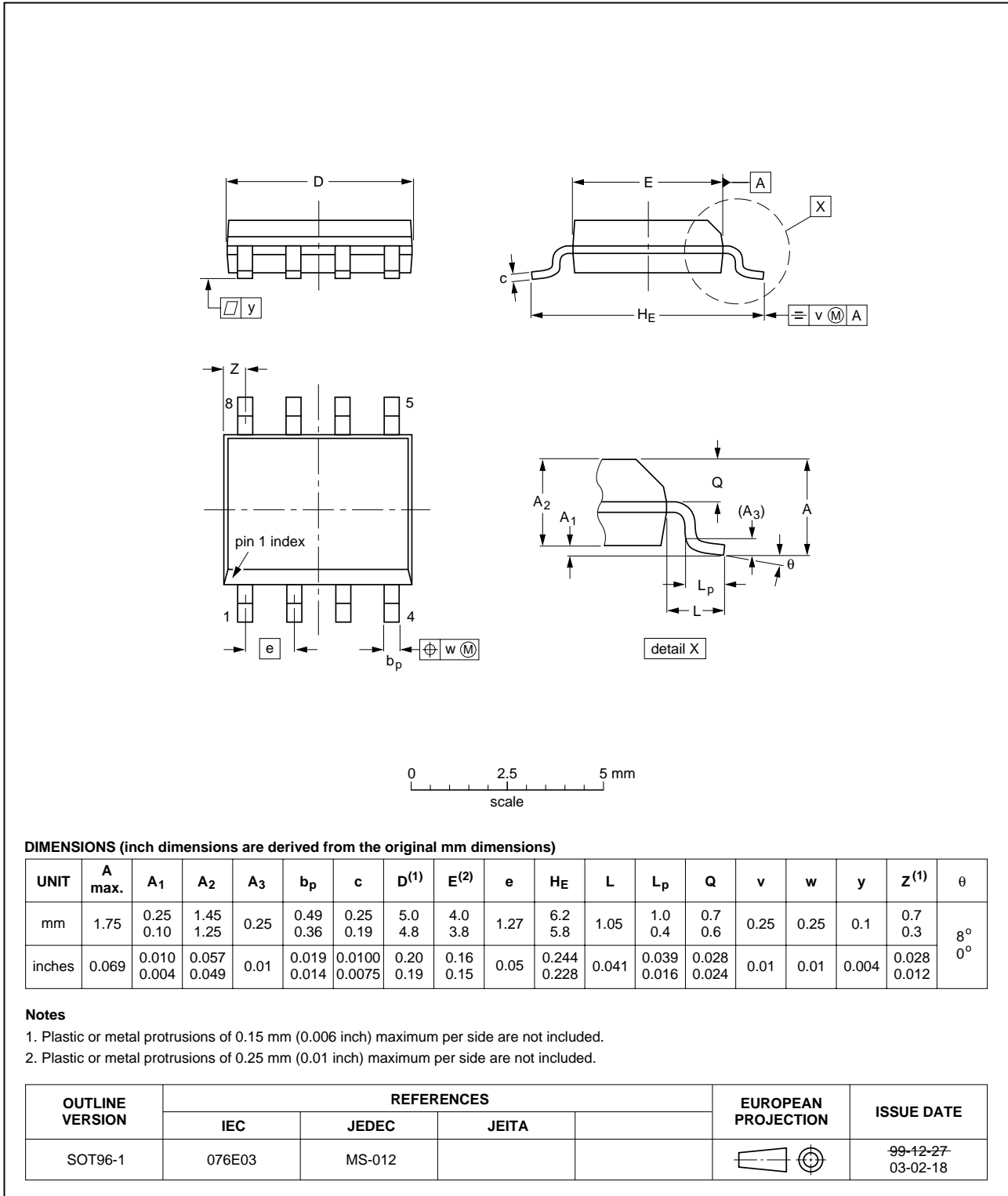


Fig 14. SOT96-1 (SO8).

8. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
02	20040217	-	Product data (9397 750 12899) Modifications: <ul style="list-style-type: none"> • Updated to latest standards. • Section 3 “Ordering information” added. • Section 5 “Thermal characteristics” clarification of thermal resistance table. • Section 6 “Characteristics” typical R_{DSon} value improved. • Section 6 “Characteristics” typical $Q_{g(tot)}$, Q_{gs} and Q_{gd} values improved. • Section 6 “Characteristics” $t_{d(on)}$, t_r, $t_{d(off)}$ and t_f conditions and typical values modified. • Section 6 “Characteristics” V_{SD} conditions, and typical value modified. • Section 6 “Characteristics” t_{rr} conditions and typical value modified • Section 6 “Characteristics” Figure 5, 6, 7, 11, 12 and 13 modified.
01	20010713	-	Product data (9397 750 08412)

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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For sales office addresses, send e-mail to: sales.addresses@www.semiconductors.philips.com.

Fax: +31 40 27 24825

Contents

1	Product profile	1
1.1	Description	1
1.2	Features	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	1
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
5.1	Transient thermal impedance	4
6	Characteristics	5
7	Package outline	9
8	Revision history	10
9	Data sheet status	11
10	Definitions	11
11	Disclaimers	11

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