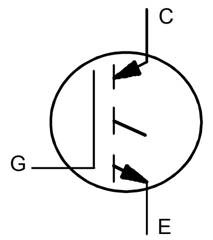
INSULATED GATE BIPOLAR TRANSISTOR

V_{CES} = 1200V

$I_{C(Nominal)}$ = 75A

$T_{J(max)}$ = 175°C

$V_{CE(on)}$ typ = 1.6V @ I_C= 75A



n-channel

G	C	E
Gate	Collector	Emitter

Applications

- Medium Power Drives
- UPS
- HEV Inverter
- Welding
- Induction Heating

Features →	Benefits
Low $V_{CE(ON)}$ and switching Losses	High efficiency in a wide range of applications
Square RBSOA	Rugged Transient Performance
Maximum Junction Temperature 175°C	Increased Reliability
Positive $V_{CE\ (ON)}$ Temperature Coefficient	Excellent current sharing in parallel operation
Integrated Gate Resistor	

Base part number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRG7CH73UEF-R	Die on film	Wafer	1	IRG7CH73UEF-R

Mechanical Parameter

Die Size	9.0 x 9.0	mm^2
Minimum Street Width	75	µm
Emiter Pad Size (Included Gate Pad)	See Die Drawing	mm^2
Gate Pad Size	1.0 x 1.7	
Area Total / Active	81/57.7	
Thickness	120	µm
Wafer Size	200	mm
Flat Position	0	Degrees
Maximum-Possible Chips per Wafer	319 pcs	
Passivation Front side	Silicon Nitride	
Front Metal	Al, Si (4µm)	
Backside Metal	Al- Ti - Ni- Ag (1kA°-1kA°-4kA°-6kA°)	
Die Bond	Electrically conductive epoxy or solder	
Reject Ink Dot Size	0.25 mm diameter minimum	

Maximum Ratings

	Parameter	Max.	Units
V_{CE}	Collector-Emitter Voltage, T_J=25°C	1200	V
I_C	DC Collector Current	①	A
I_{LM}	Clamped Inductive Load Current ②	300	A
V_{GE}	Gate Emitter Voltage	± 30	V
T_J, T_{STG}	Operating Junction and Storage Temperature	-40 to +175	°C

Static Characteristics (Tested on wafers) . T_J=25°C

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	1200	—	—	V	V_{GE} = 0V, I_C = 100μA ③
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	—	2.0		V_{GE} = 15V, I_C = 75A, T_J = 25°C
$V_{GE(th)}$	Gate-Emitter Threshold Voltage	3.0	—	6.0		I_C = 3.5mA , V_{GE} = V_{CE}
I_{CES}	Zero Gate Voltage Collector Current	—	1.0	25	μA	V_{CE} = 1200V, V_{GE} = 0V
I_{GES}	Gate Emitter Leakage Current	—	—	± 400	nA	V_{CE} = 0V, V_{GE} = ±30V
$R_{G\ INTERNAL}$	Internal Gate Resistance	1.9	2.5	3.1	Ω	

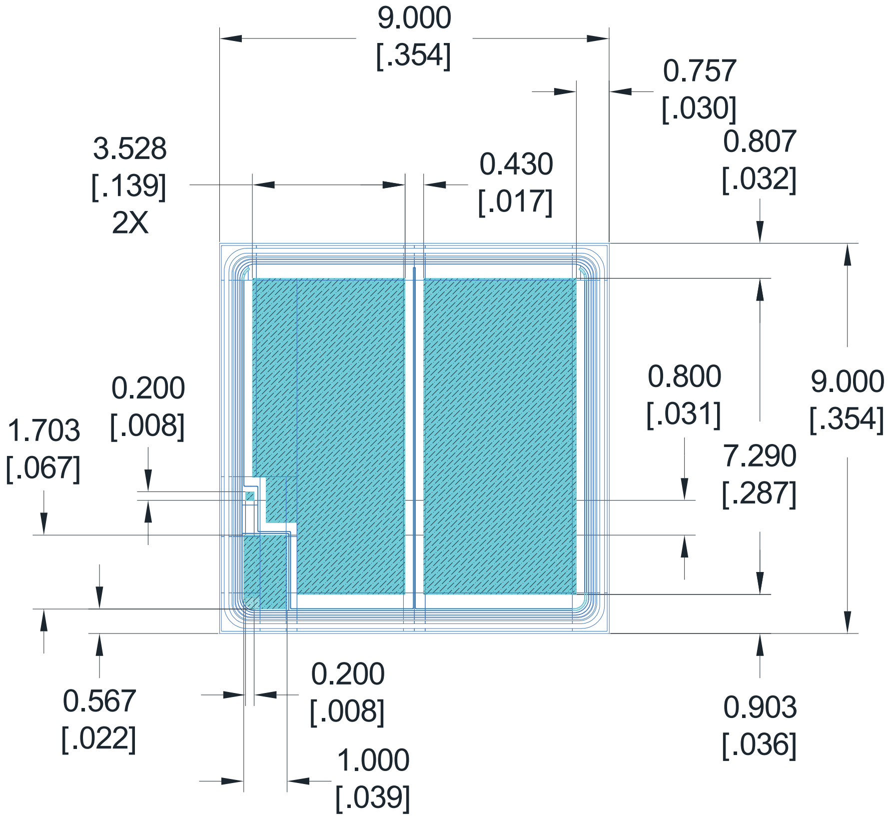
Electrical Characteristics (Not subject to production test- Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{CE(sat)}$	Collector-to-Emitter Saturated Voltage	—	1.6	—	V	V_{GE} = 15V, I_C = 75A , T_J = 25°C ④
		—	2.0	—		V_{GE} = 15V, I_C = 75A , T_J = 175°C④
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				T_J = 175°C, I_C = 300A V_{CC} = 960V, Vp ≤1200V Rg = 5Ω, V_{GE} = +20V to 0V
C_{iss}	Input Capacitance	—	10000	—	pF	V_{GE} = 0V
C_{oss}	Output Capacitance	—	330	—		V_{CE} = 30V
C_{rss}	Reverse Transfer Capacitance	—	250	—		*ƒ* = 1.0MHz,
Q_g	Total Gate Charge (turn-on)	—	540	—	nC	I_C = 75A ⑥
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	80	—		V_{GE} = 15V
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	230	—		V_{CC} = 600V

Switching Characteristics (Inductive Load-Not subject to production test-Verified by design/characterization)

	Parameter	Min.	Typ.	Max.	Units	Conditions ⑥⑦
$t_{d(on)}$	Turn-On delay time	—	90	—	ns	I_C = 75A, V_{CC} = 600V
t_r	Rise time	—	70	—		R_G = 5Ω, V_{GE}=15V, L=200μH
$t_{d(off)}$	Turn-Off delay time	—	580	—		T_J = 25°C
t_f	Fall time	—	50	—		
$t_{d(on)}$	Turn-On delay time	—	80	—		I_C = 75A, V_{CC} = 600V
t_r	Rise time	—	70	—		R_G = 5Ω, V_{GE}=15V, L= 200μH
$t_{d(off)}$	Turn-Off delay time	—	735	—		T_J = 175°C
t_f	Fall time	—	150	—		

Die Drawing



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
2. CONTROLLING DIMENSION: INCHES
3. DIE WIDTH AND LENGTH TOLERANCE: -0.0508 [.002]
4. DIE THICKNESS = 0.120 [.0047]

REFERENCE: IRG7CH73UB-R

Notes:

① The current in the application is limited by T_{JMax} and the thermal properties of the assembly.

② V_{CC} = 80% (V_{CES}), V_{GE} = 20V, L = 200µH, R_G = 5Ω.

③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely

④ Die Level Characterization

⑤ Not subject to production test-Verified by design / characterization

⑥ Pulse width limited by junction temperature

⑦ Values influenced by parasitic L and C in measurement

Additional Testing and Screening

For Customers requiring product supplied as Known Good Die (KGD) or requiring specific die level testing, please contact your local IR Sales.

Shipping

Sawn Wafer on Film. Please contact your local IR sales office for non– standard shipping options

Handling

- Product must be handled only at ESD safe workstations. Standard ESD precautions and safe work environments are as defined in MIL-HDBK-263.
- Product must be handled only in a class 10,000 or better-designated clean room environment.
- Singulated die are not to be handled with tweezers. A vacuum wand with a non-metallic ESD protected tip should be used.

Wafer/Die Storage

- Proper storage conditions are necessary to prevent product contamination and/or degradation after shipment.
- Note: To reduce the risk of contamination or degradation, it is recommended that product not being used in the assembly process be returned to their original containers and resealed with a vacuum seal process.
- Sawn wafers on a film frame are intended for immediate use and have a limited shelf life.

Further Information

For further information please contact your local IR Sales office or email your enquiry to http://die.irf.com

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