

# DATA SHEET

## **CBTS3306**

Dual bus switch with Schottky diode clamping

Product data

2001 Nov 08

File under Integrated Circuits — ICL03

# Dual bus switch with Schottky diode clamping

# CBTS3306

## FEATURES

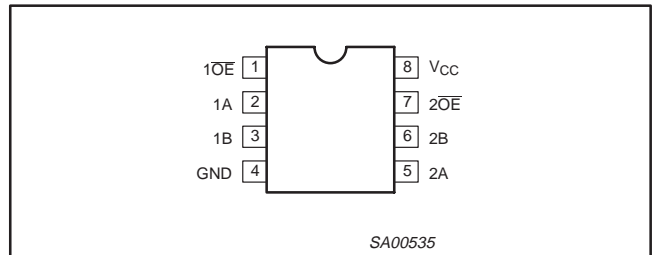
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Package options include plastic small outline (SO) and thin shrink small outline (TSSOP)
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101

## DESCRIPTION

The CBTS3306 Dual FET Bus Switch features independent line switches with Schottky diodes on the I/Os to clamp undershoot. Each switch is disabled with the associated Output Enable ( $\overline{OE}$ ) input is high.

The CBTS3306 is characterized for operation from -40 to +85 °C.

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 7	$1\overline{OE}$ , $2\overline{OE}$	Output enable
2, 5	1A, 2A	A port inputs
3, 6	1B, 2B	B port outputs
4	GND	Ground (0 V)
8	$V_{CC}$	Positive supply voltage

## QUICK REFERENCE DATA

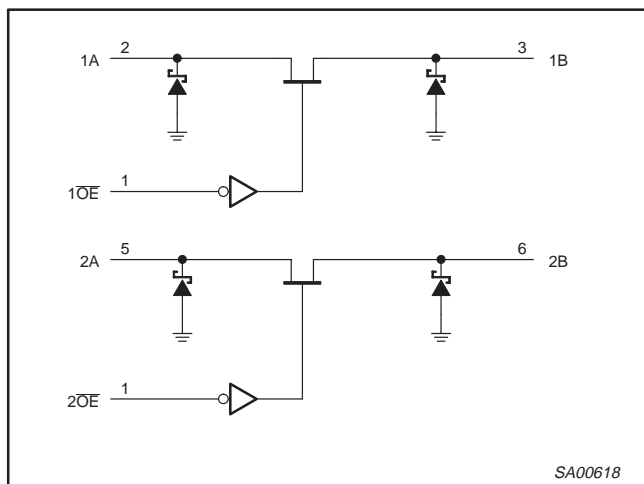
SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25\text{ °C}$ ; $GND = 0\text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay A to B or B to A	$C_L = 50\text{ pF}$ ; $V_{CC} = +5.0\text{ V} \pm 0.5\text{ V}$	0.25 (MAX)	ns
$C_{IO(OFF)}$	Port off capacitance	$V_O = 3\text{ V}$ or 0; $\overline{OE} = V_{CC}$	7.60	pF
$I_{CC}$	Quiescent supply current	$V_{CC} = 5.5\text{ V}$ ; $I_O = 0$ , $V_I = V_{CC}$ or GND	3	$\mu\text{A}$

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
8-pin plastic SO	-40 to 85 °C	CBTS3306D	SOT96-1
8-pin plastic TSSOP	-40 to 85 °C	CBTS3306PW	SOT530-1

Standard packing quantities and other packaging data is available at [www.philipslogic.com/packaging](http://www.philipslogic.com/packaging).

## LOGIC DIAGRAM (positive logic)



## FUNCTION TABLE

INPUT	FUNCTION
$\overline{OE}$	
L	A port = B port
H	Disconnect

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**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>** $T_{amb} = -40$  to  $+85$  °C, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$V_I$	DC input voltage <sup>2</sup>		-0.5 to +7.0	V
$I_{OUT}$	DC output current		128	mA
$I_{IK}$	Diode current	$V_{I/O} < 0$	-50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- The package thermal impedance is calculated in accordance with JESD 51.

**RECOMMENDED OPERATING CONDITIONS<sup>1</sup>**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.0	—	V
$V_{IL}$	Low-level Input voltage	—	0.8	V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

**NOTE:**

- All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation.

**DC ELECTRICAL CHARACTERISTICS** $T_{amb} = -40$  to  $+85$  °C, unless otherwise specified.

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS			UNIT
				$T_{amb} = -40$ to $+85$ °C			
				MIN	TYP <sup>1</sup>	MAX	
$V_{IK}$	Input clamp voltage	A or B input	$V_{CC} = 4.5$ V; $I_I = -18$ mA	—	—	-0.7	V
		Control inputs	$V_{CC} = 4.5$ V; $I_I = -18$ mA	—	—	-1.2	
$I_I$	Input leakage current		$V_{CC} = 5.5$ V; $V_I =$ GND or 5.5 V	—	—	$\pm 1$	$\mu$ A
$I_{CC}$	Quiescent supply current		$V_{CC} = 5.5$ V; $I_O = 0$ , $V_I = V_{CC}$ or GND	—	—	3	$\mu$ A
$V_P$	Output high pass voltage		$V_O = V_{CC} = 5.0$ V; $I_I = -100$ mA	3.4	3.6	3.9	V
$\Delta I_{CC}$	Additional supply current per input pin <sup>2</sup>		$V_{CC} = 5.5$ V, one input at 3.4 V, other inputs at $V_{CC}$ or GND	—	—	2.5	mA
$C_I$	Control pin capacitance		$V_I = 3$ V or 0	—	3.25	—	pF
$C_{I(OFF)}$	Port off capacitance		$V_O = 3$ V or 0; $\overline{OE} = V_{CC}$	—	7.60	—	pF
$r_{on}$ <sup>3</sup>	On-resistance		$V_{CC} = 4.5$ V; $V_I = 0$ V; $I_I = 64$ mA	—	3.4	5	$\Omega$
			$V_{CC} = 4.5$ V; $V_I = 0$ V; $I_I = 30$ mA	—	3.4	5	$\Omega$
			$V_{CC} = 4.5$ V; $V_I = 2.4$ V; $I_I = 15$ mA	—	6.8	7.5	$\Omega$

**NOTES:**

- All typical values are at  $V_{CC} = 5$  V,  $T_{amb} = 25$  °C.
- This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND.
- Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

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## AC CHARACTERISTICS

$T_{amb} = -40$  to  $+85$  °C;  $C_L = 50$  pF

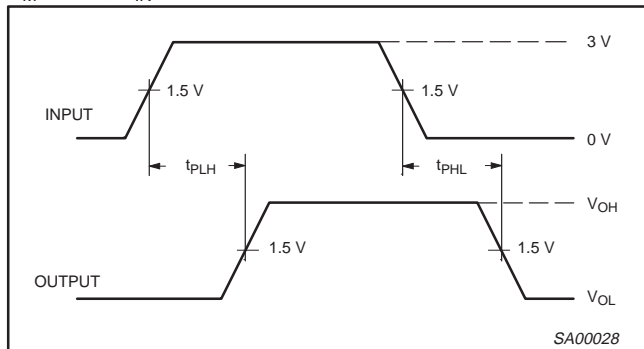
SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				$V_{CC} = +5.0 V \pm 0.5 V$		
				MIN	MAX	
$t_{pd}$	Propagation delay <sup>1</sup>	A or B	B or A	—	0.25	ns
$t_{en}$	Output enable time to High and Low level	$\overline{OE}$	A or B	1.8	5	ns
$t_{dis}$	Output disable time from High and Low level	$\overline{OE}$	A or B	1	5	ns

**NOTE:**

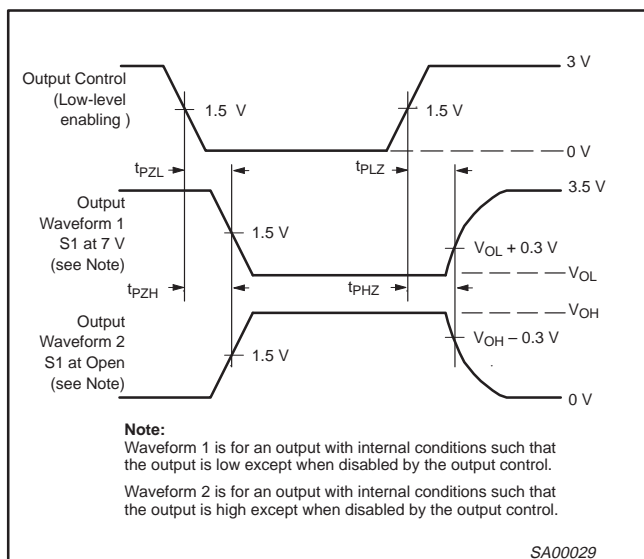
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

## AC WAVEFORMS

$V_M = 1.5 V$ ,  $V_{IN} = GND$  to  $3.0 V$



**Waveform 1. Input to Output Propagation Delays**



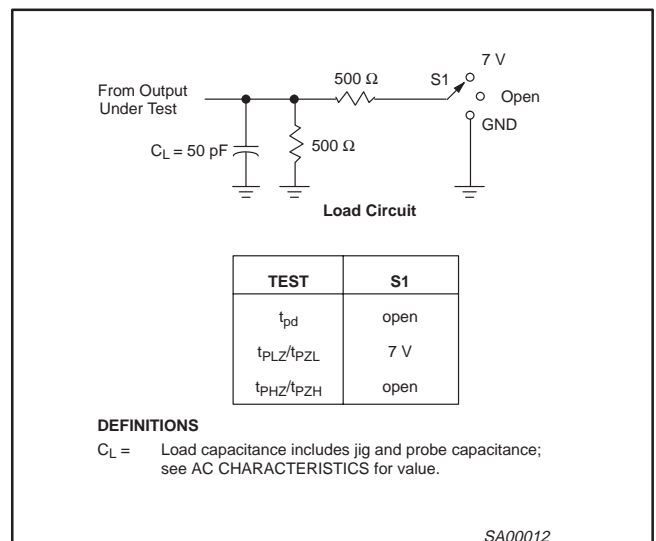
**Note:**  
 Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

**Waveform 2. 3-State Output Enable and Disable Times**

**NOTES:**

1.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
2.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
3.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

## TEST CIRCUIT AND WAVEFORMS



**NOTES:**

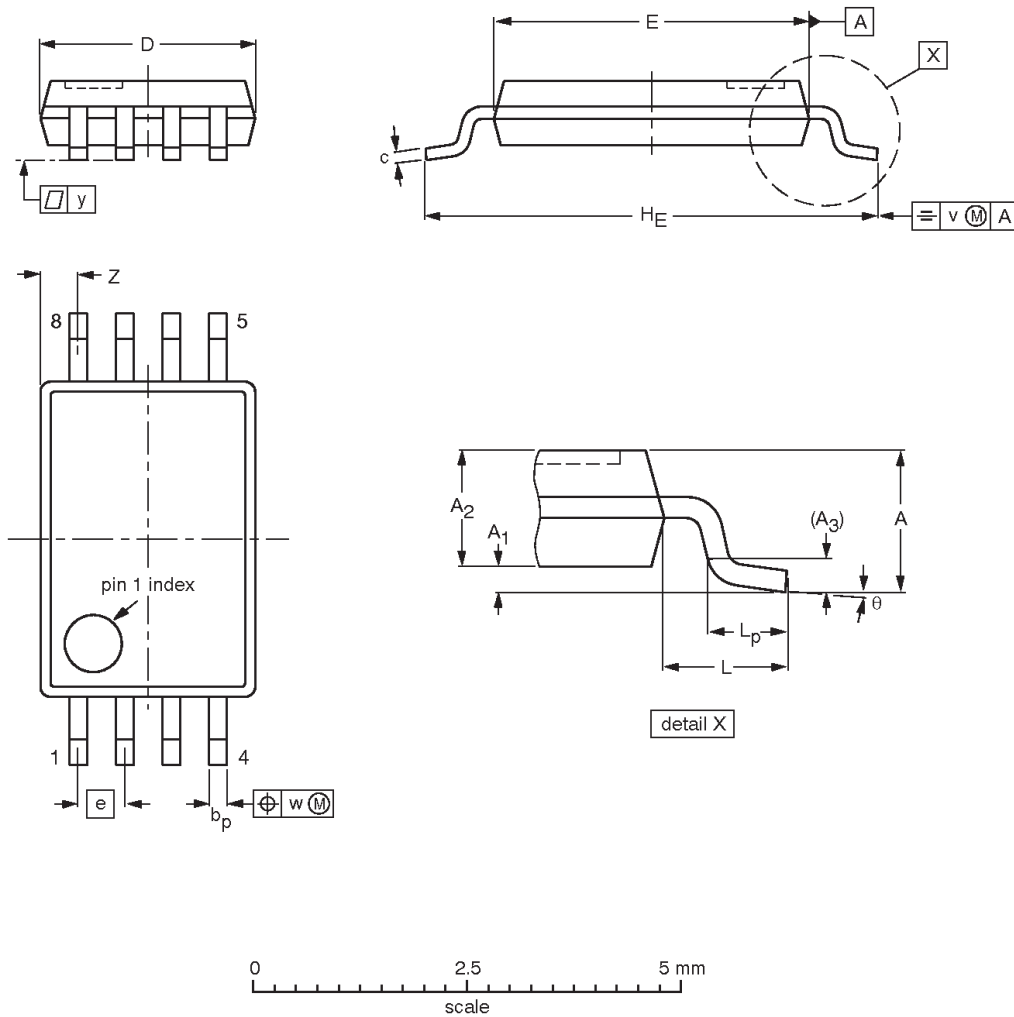
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
2. The outputs are measured one at a time with one transition per measurement.

# Dual bus switch with Schottky diode clamping

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**TSSOP8: plastic thin shrink small outline; 8 leads; body width 4.4 mm**

**SOT530-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.10 2.90	4.50 4.30	0.65	6.50 6.30	0.94	0.70 0.50	0.10	0.10	0.10	0.70 0.35	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

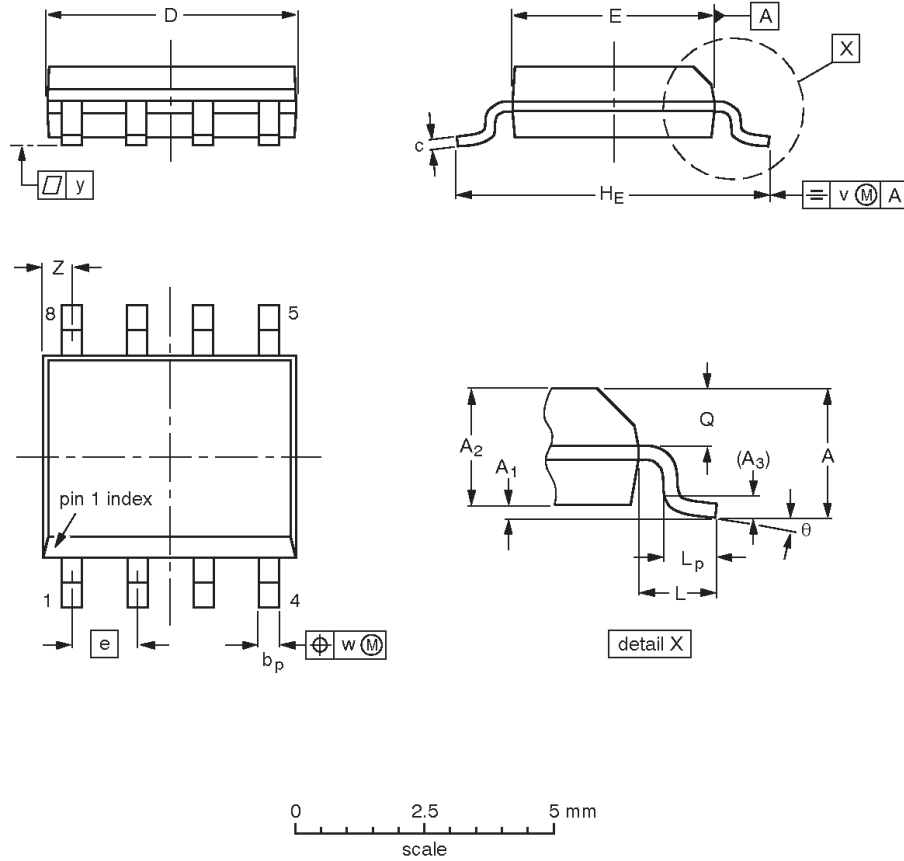
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT530-1		MO-153				99-12-27 00-02-24

# Dual bus switch with Schottky diode clamping

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**S08:** plastic small outline package; 8 leads; body width 3.9 mm

**SOT96-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22 99-12-27

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**NOTES**

## Dual bus switch with Schottky diode clamping

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Date of release: 11-01

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